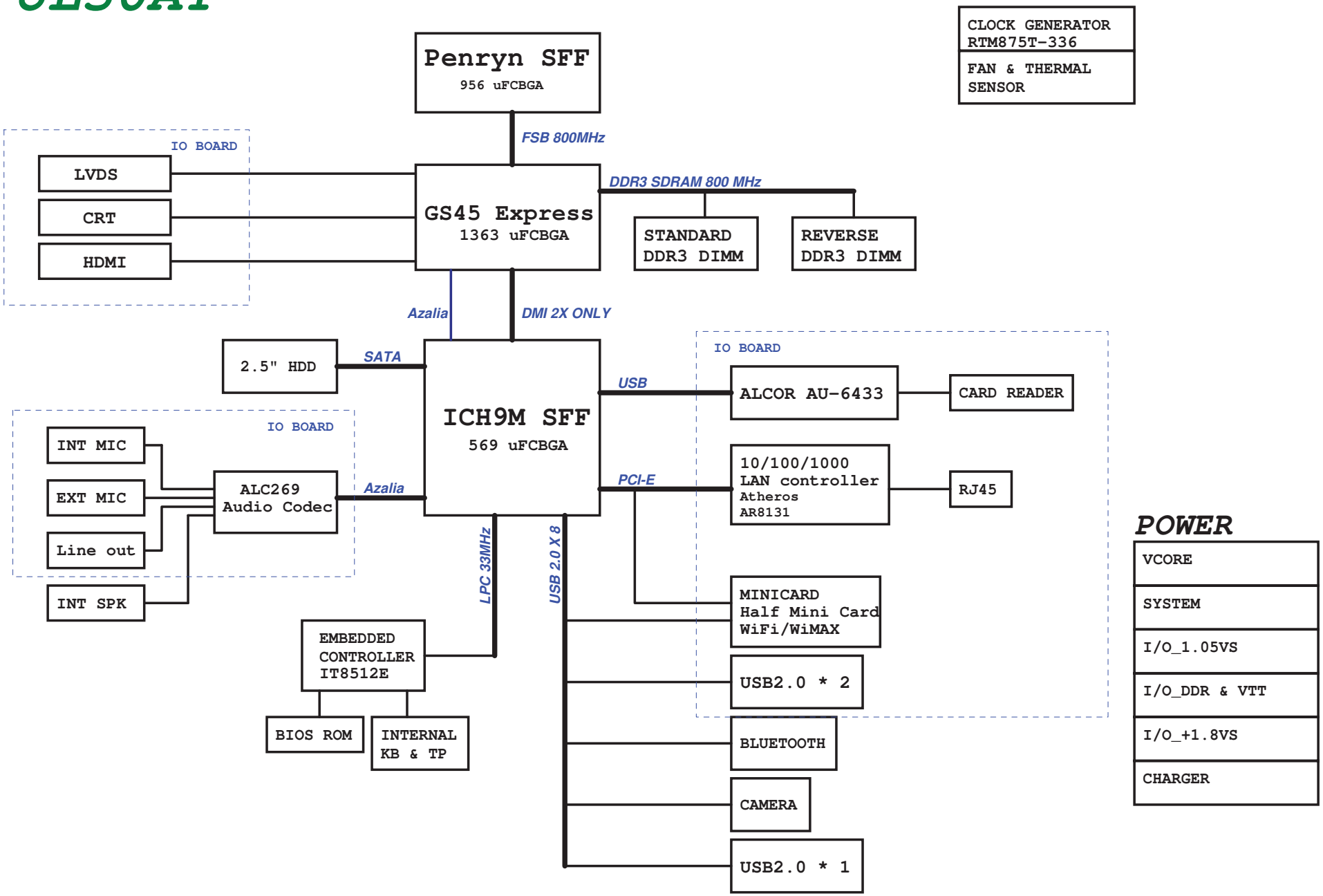
UL50AT



<Variant Name>

ASUSTeK COMPUTER INC.

Title : Block Diagram

Engineer: Jack Hsu

Size	Project Name	Rev
Custom	UL50AT	2.0

Date: Friday, October 16, 2009 Sheet 1 of 97

UL50A SCHEMATIC Revision 2.1

PAGE	Content

SYSTEM PAGE REF.

PAGE	Content

POWER PAGE REF.

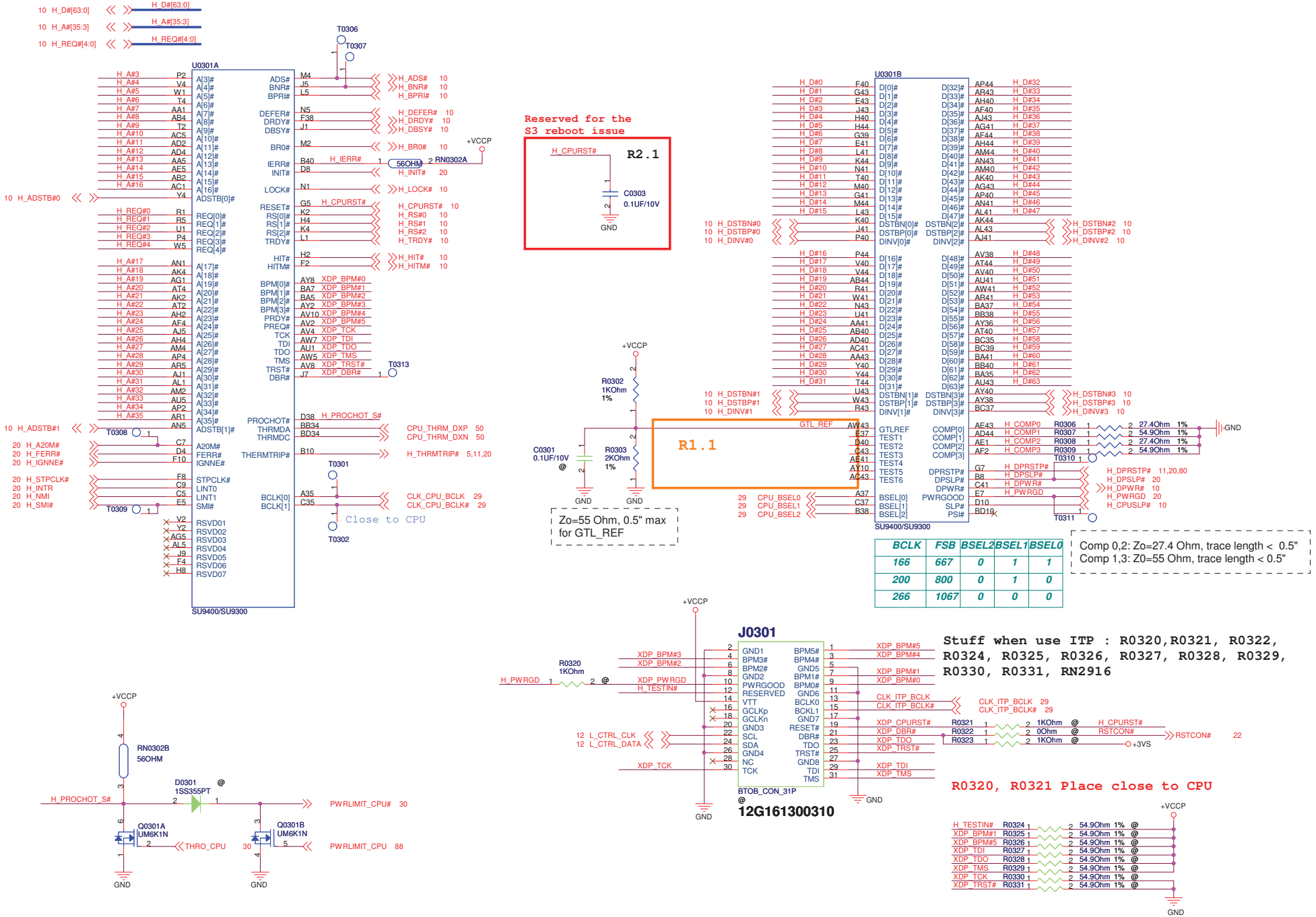
<Variant Name>

Title : Page Reference

ASUSTeK COMPUTER INC. Engineer: Jack Hsu

Size	Project Name	Rev
Custom	UL50AT	2.0

Date: Friday, October 16, 2009 Sheet 2 of 97



<Variant Name>

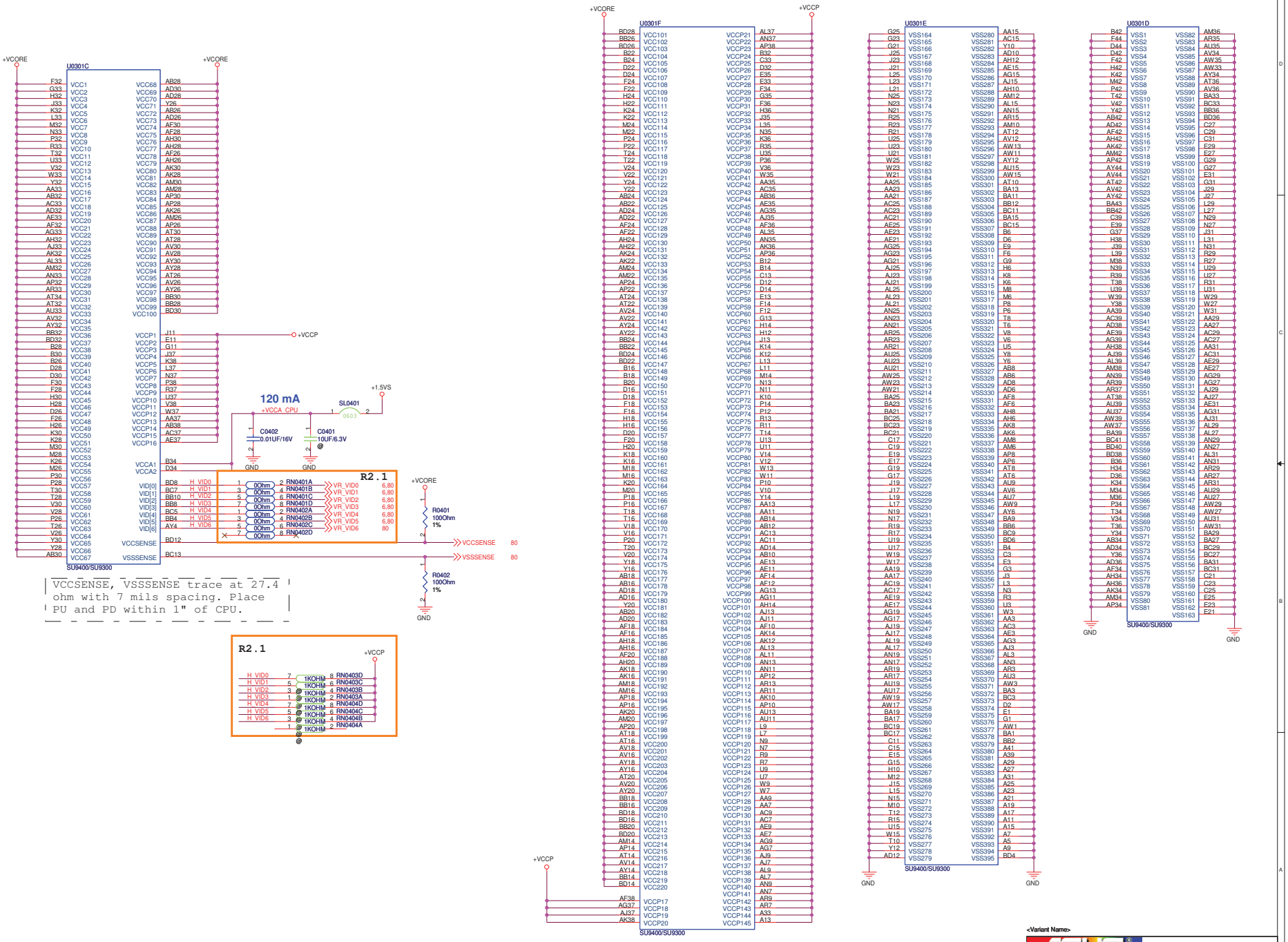
ASUSTeK COMPUTER INC.

Title : PENRYN ULV FSB

Engineer: Jack Hsu

Size	Project Name	Rev
Custom	UL50AT	2.0

Date: Friday, October 16, 2009 Sheet 3 of 97



<Variant Name>

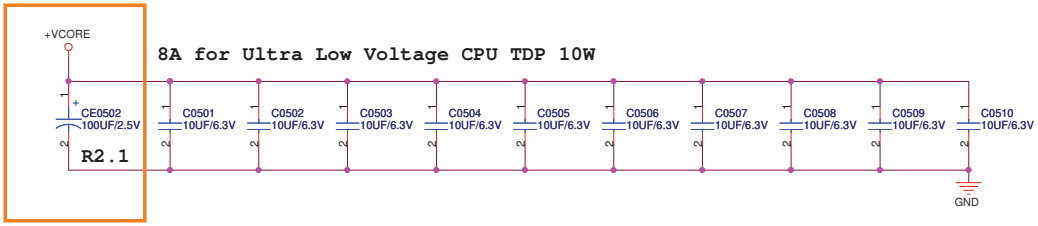
Title : PENRYN ULV POWER

ASUSTeK COMPUTER INC.

Engineer: Jack Hsu

Size	Project Name	Rev
C	UL50AT	2.0

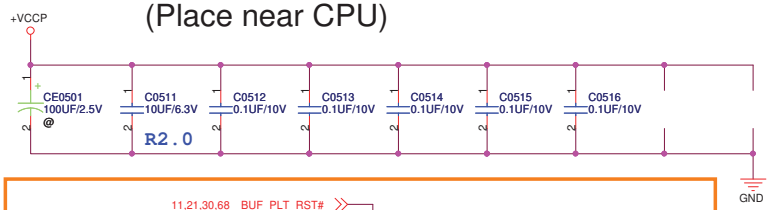
Date: Friday, October 16, 2009 Sheet 4 of 97

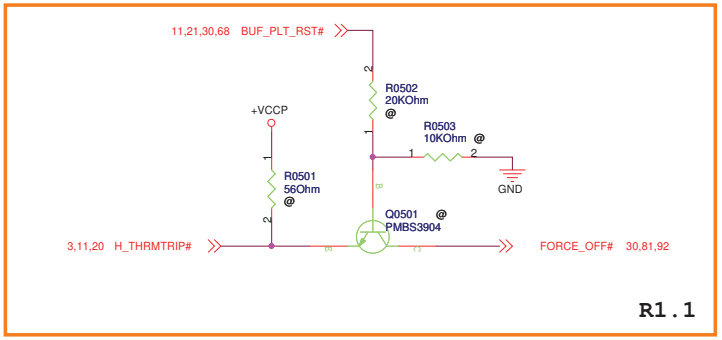


Decoupling guide from Intel

VCORE	10uF mount	*4pcs
	0.1uF mount	*5pcs
VCCP	1uF	* 12pcs
	270uF	* 1pcs
VCCA	0.01uF	* 1 pcs
	10uF	* 1 pcs

+VCCP Decoupling Capacitor (Place near CPU)





<Variant Name>

ASUSTeK COMPUTER INC.

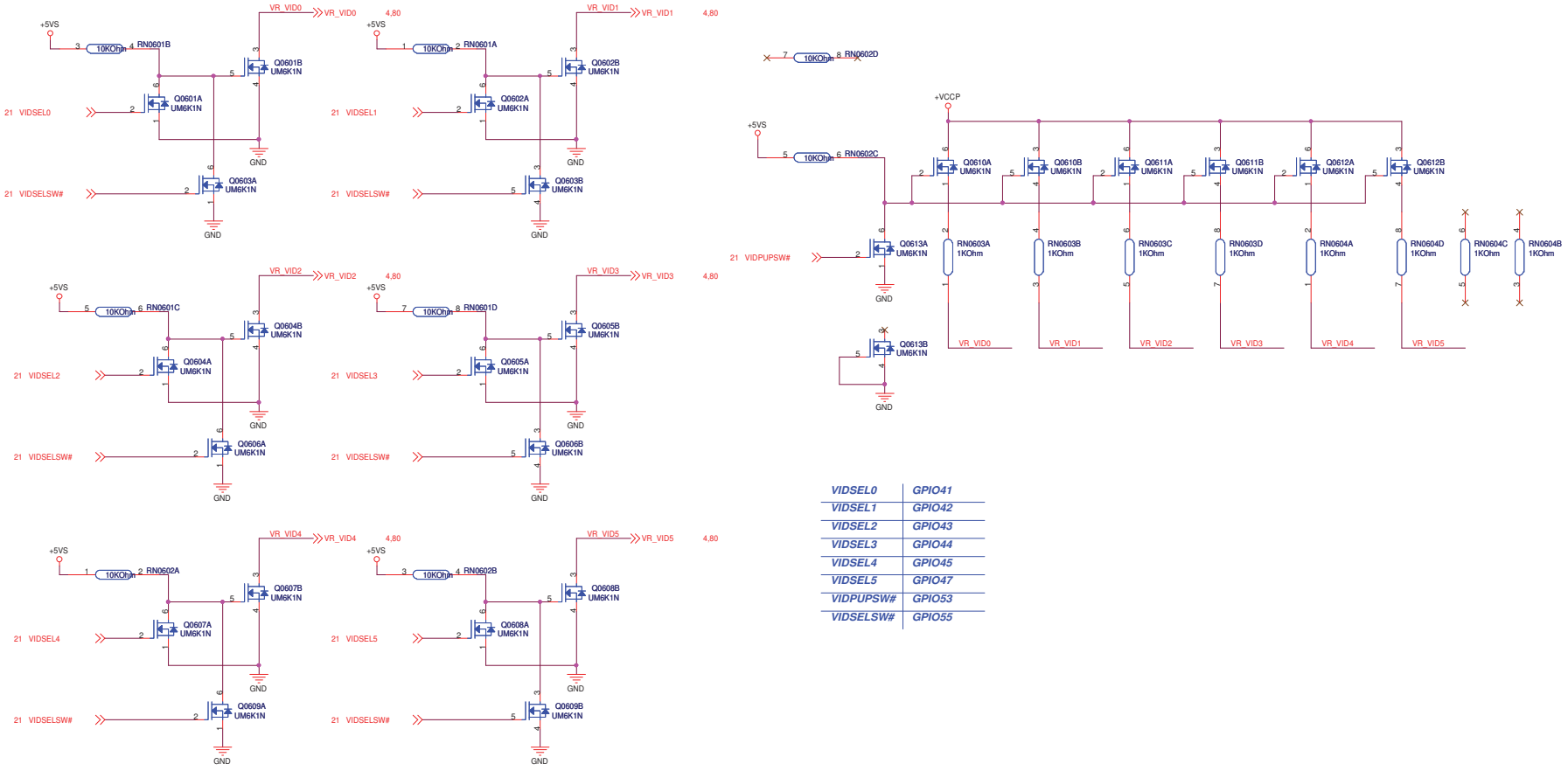
Title : CPU CAPACITORS

Engineer: Jack Hsu

Size	Project Name	Rev
Custom	UL50AT	2.0

Date: Friday, October 16, 2009 Sheet 5 of 97

R2.1



VIDSEL0	*GPIO41*
VIDSEL1	*GPIO42*
VIDSEL2	*GPIO43*
VIDSEL3	*GPIO44*
VIDSEL4	*GPIO45*
VIDSEL5	*GPIO47*
VIDPUPSW#	*GPIO53*
VIDSELSW#	*GPIO55*

<Variant Name>

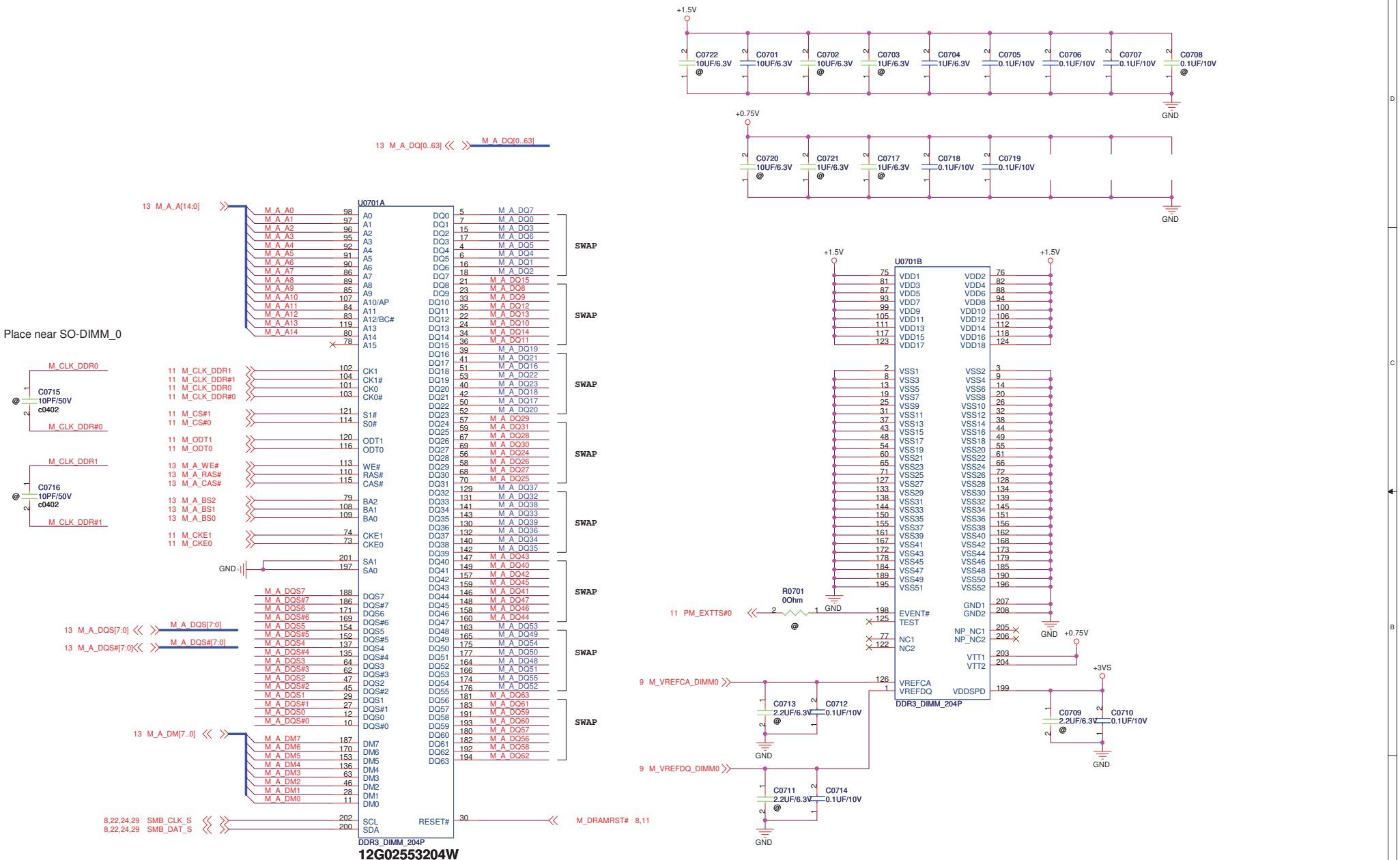
ASUSTeK COMPUTER INC.

Title :

Engineer: Jack Hsu

Size	Project Name	Rev
C	UL50AT	2.0

Date: Friday, October 16, 2009 Sheet 6 of 97

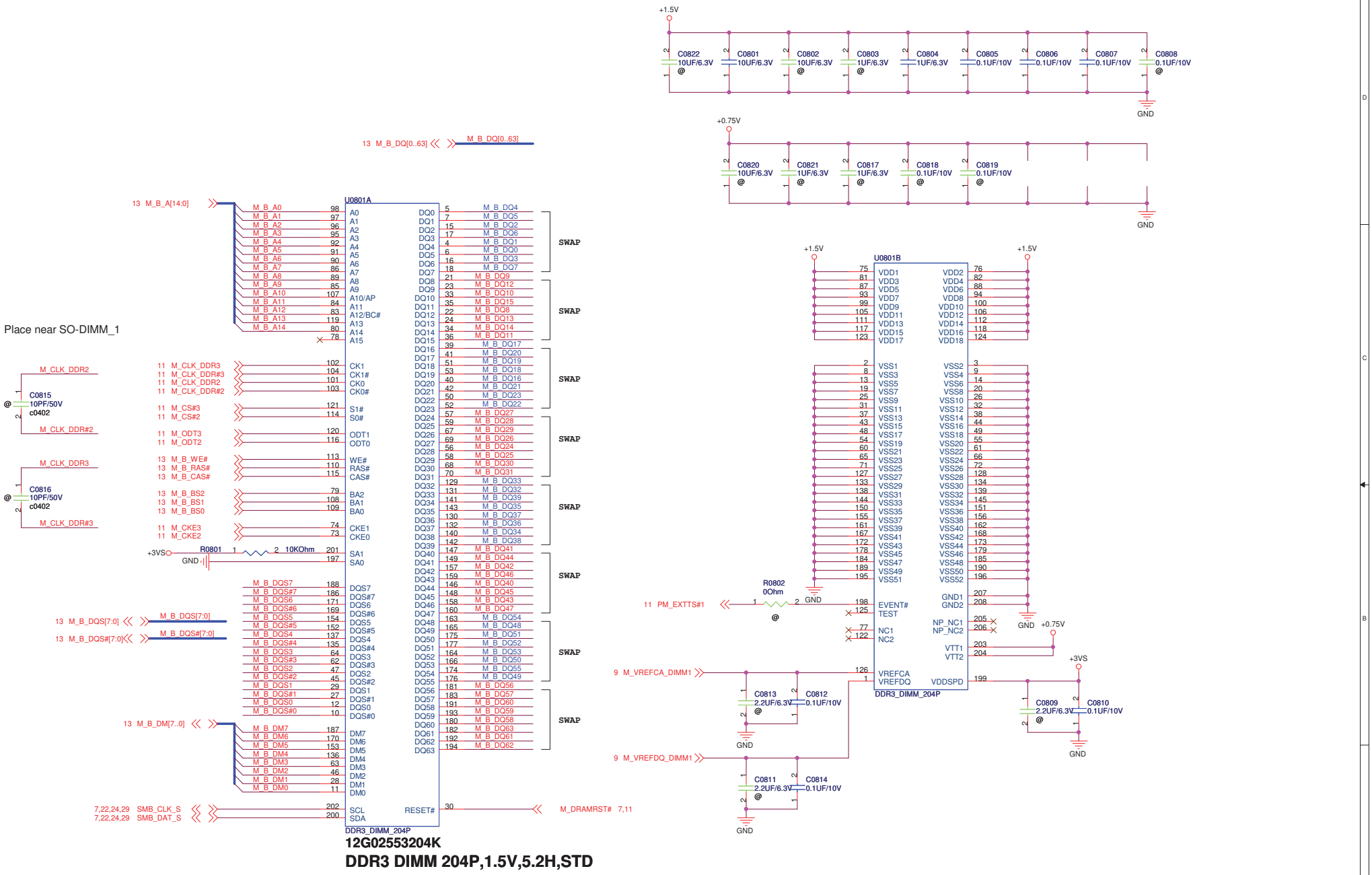


12G02553204W

DDR3 DIMM 204P,1.5V,5.2H,REV

<Variant Name>

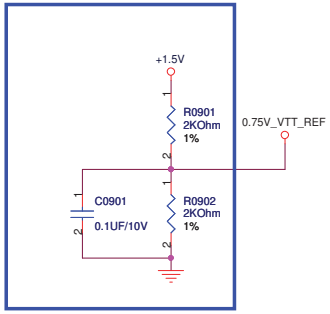
ASUSTeK COMPUTER INC.	Title : DDR3 SO-DIMM A	
	Engineer: Jack Hsu	
Size: Custom	Project Name: UL50AT	Rev: 2.0
Date: Friday, October 16, 2009	Sheet 7 of 97	

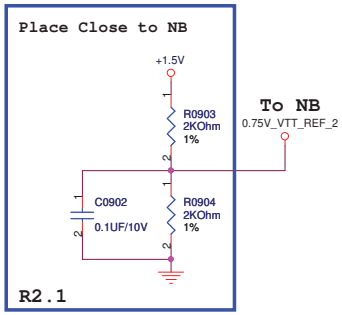


<Variant Name>

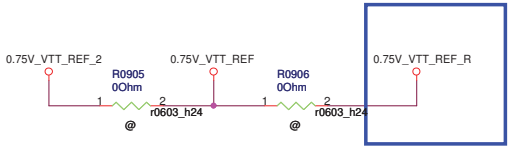
ASUSTeK COMPUTER INC.	Title : DDR3 SO-DIMM B	
	Engineer: Jack Hsu	
Size: Custom	Project Name: UL50AT	Rev: 2.0
Date: Friday, October 16, 2009	Sheet 8 of 97	

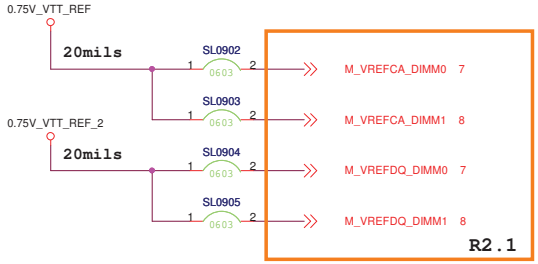
R2.1





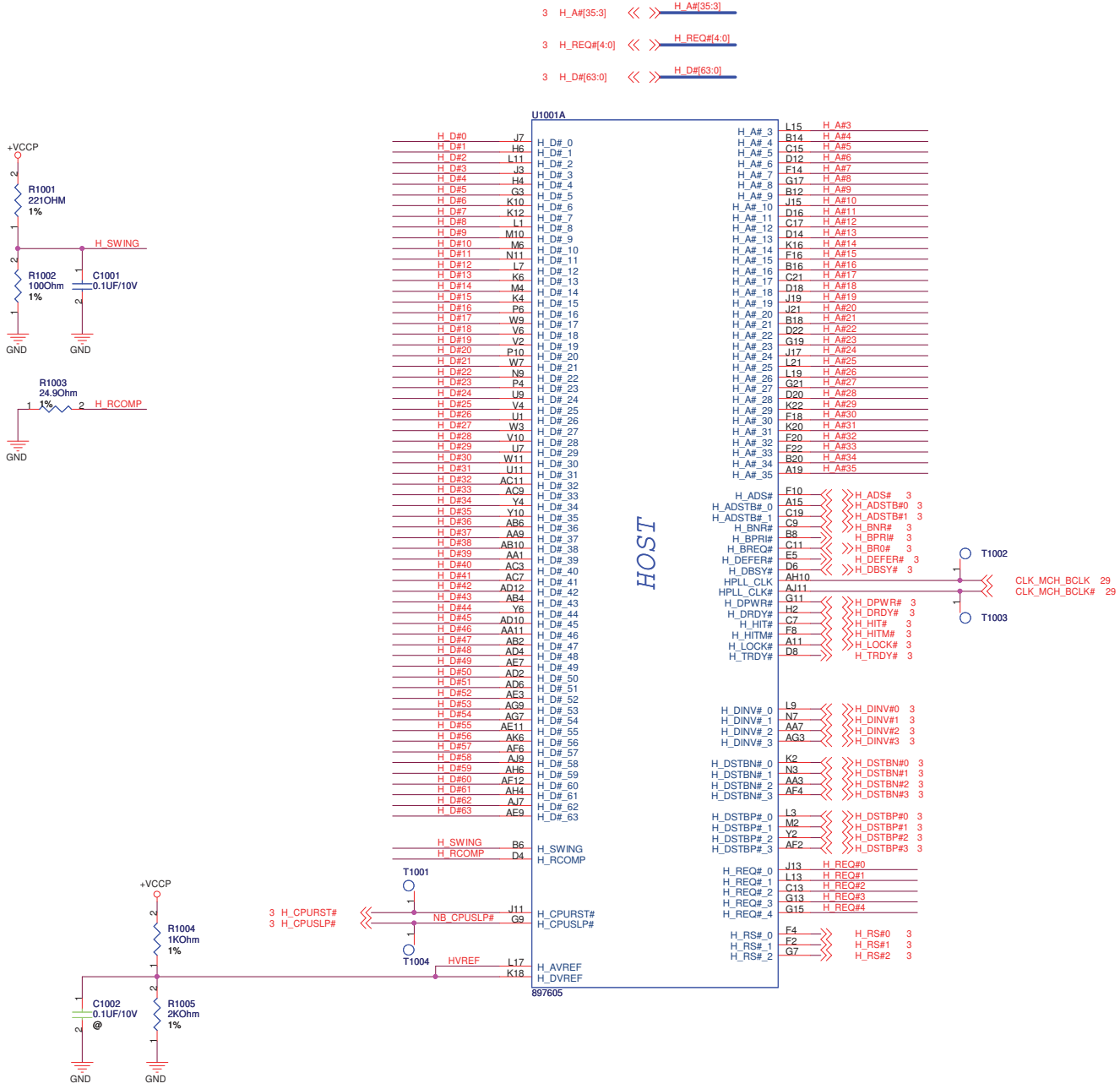
From DDR/VTT Power Circuit





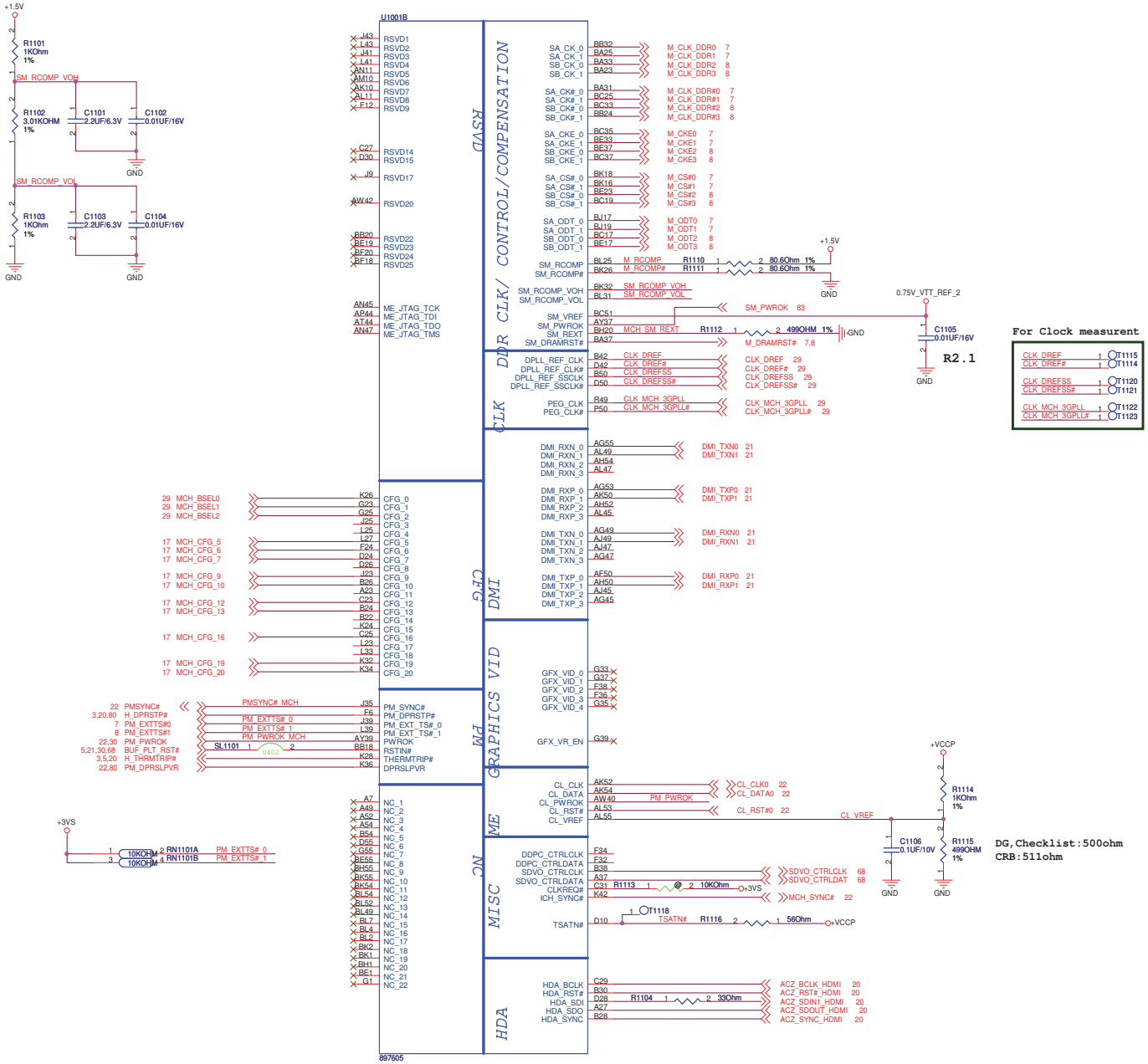
<Variant Name>

ASUSTeK COMPUTER INC.	Title : DDR3 VREF	
	Engineer: Jack Hsu	
Size: Custom	Project Name: UL50AT	Rev: 2.0
Date: Friday, October 16, 2009	Sheet 9 of 97	



<Variant Name>

ASUSTeK COMPUTER INC.	Title : NB GS45 HOST	
	Engineer: Jack Hsu	
Size: Custom	Project Name: UL50AT	Rev: 2.0
Date: Friday, October 16, 2009	Sheet 10 of 97	



<Variant Name>

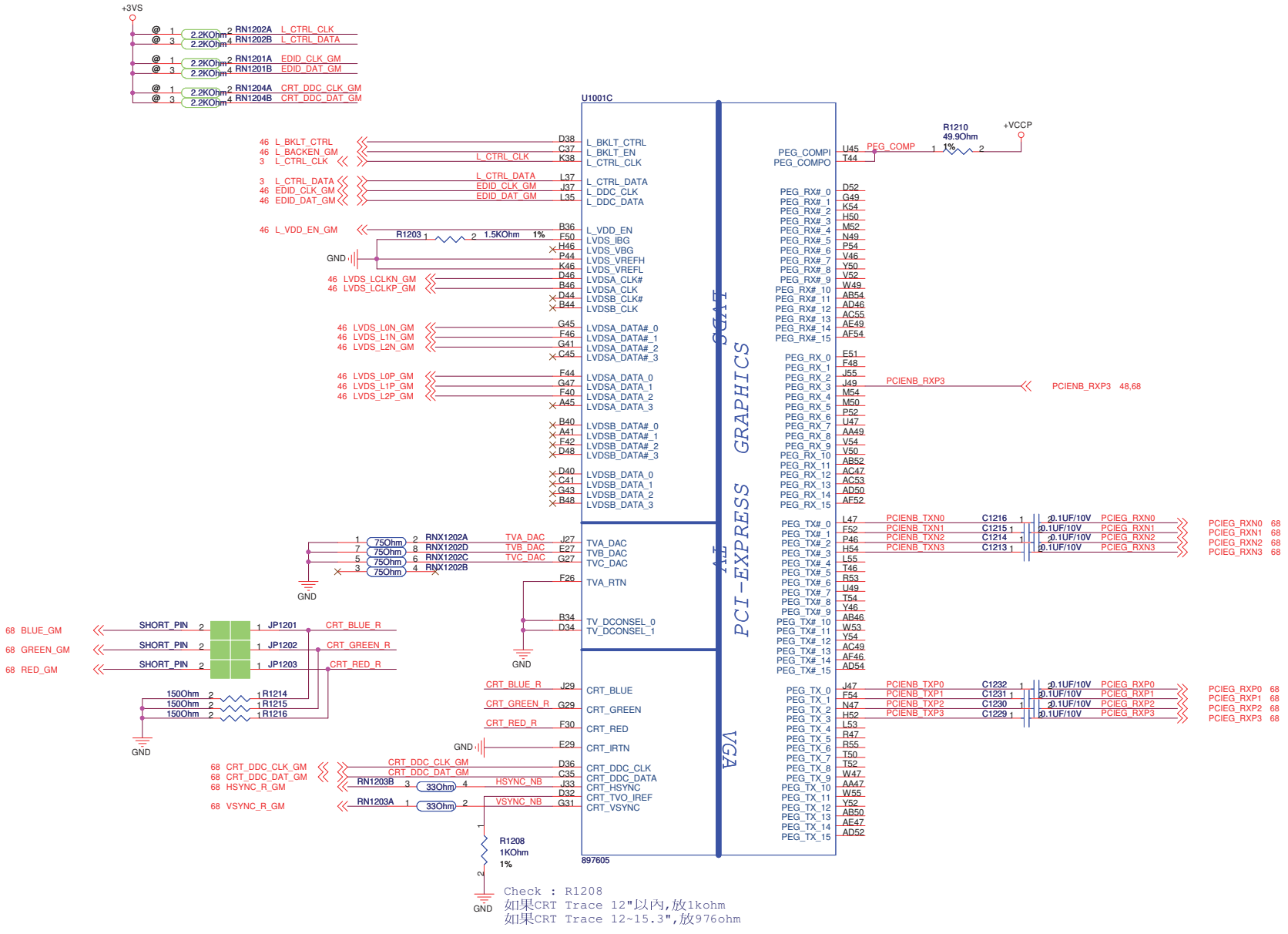
ASUSTeK COMPUTER INC.

Title : NB GS45 DMI

Engineer: Jack Hsu

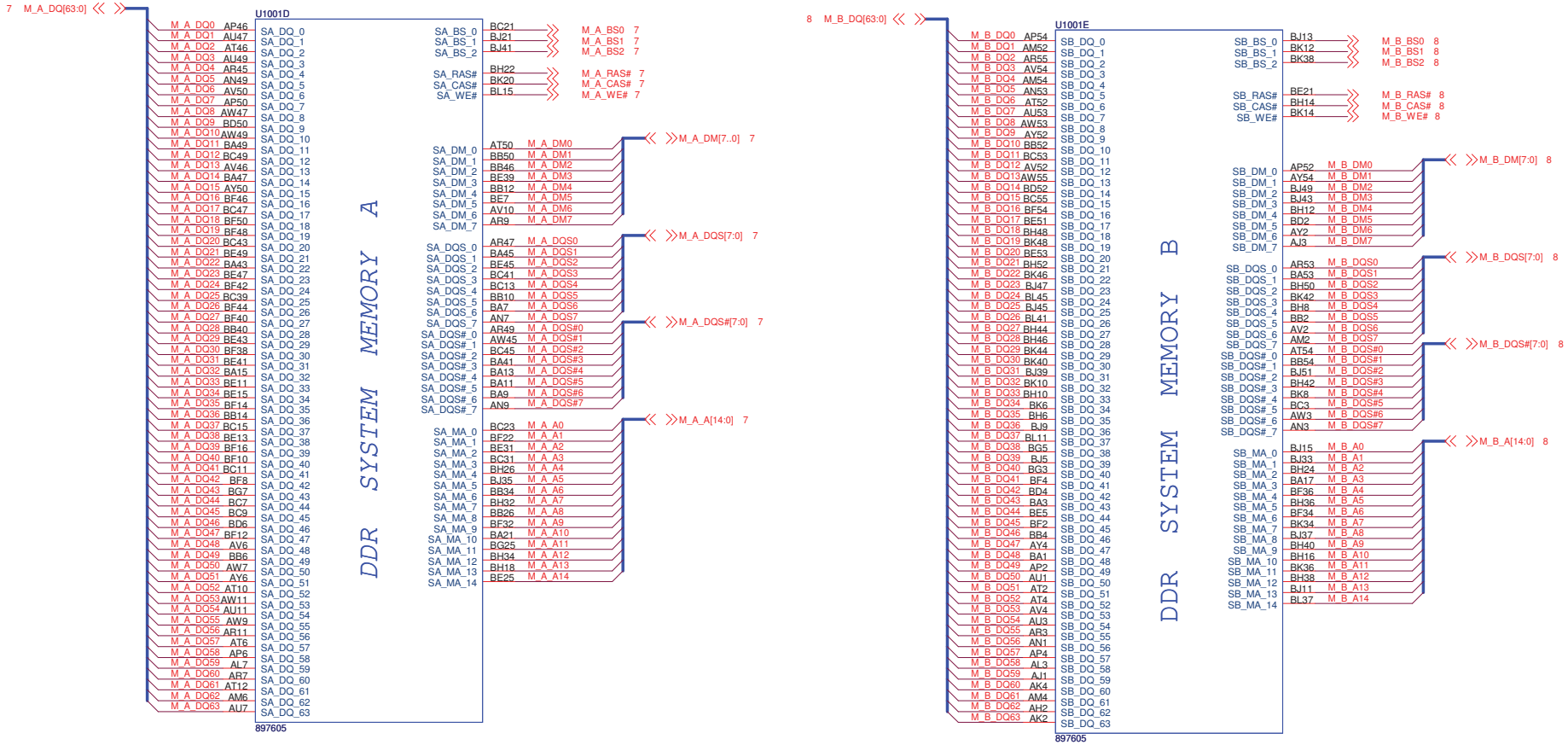
Size	Project Name	Rev
C	UL50AT	2.0

Date: Friday, October 16, 2009 Sheet 11 of 97



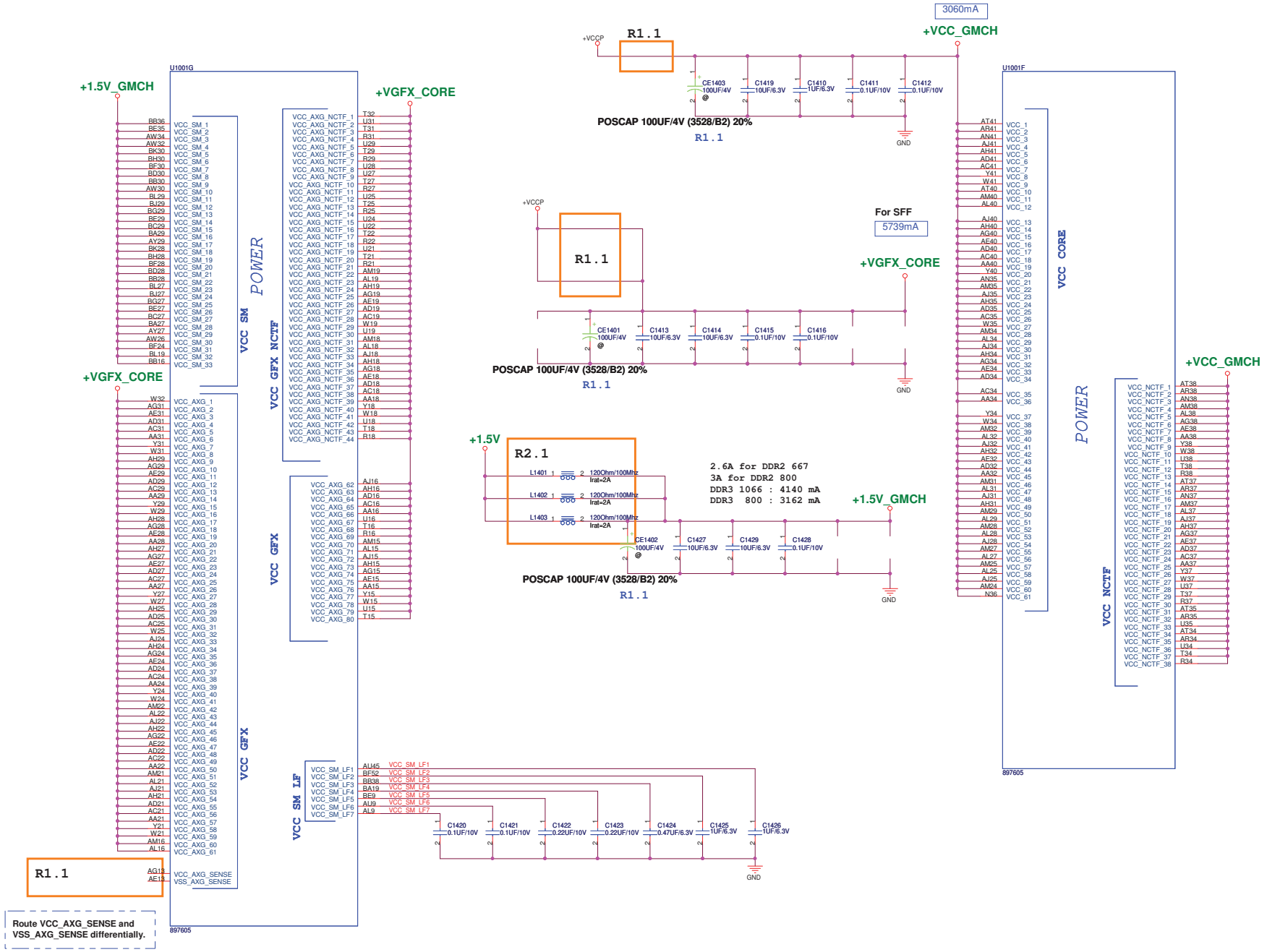
<Variant Name>

ASUSTeK COMPUTER INC.	Title : NB GS45 DISPLAY	
	Engineer: Jack Hsu	
Size: Custom	Project Name: UL50AT	Rev: 2.0
Date: Friday, October 16, 2009	Sheet 12 of 97	



<Variant Name>

ASUSTeK COMPUTER INC.	Title : NB GS45 DDR3 BUS	
	Engineer: Jack Hsu	
Size: Custom	Project Name: UL50AT	Rev: 2.0
Date: Friday, October 16, 2009	Sheet 13 of 97	



<Variant Name>

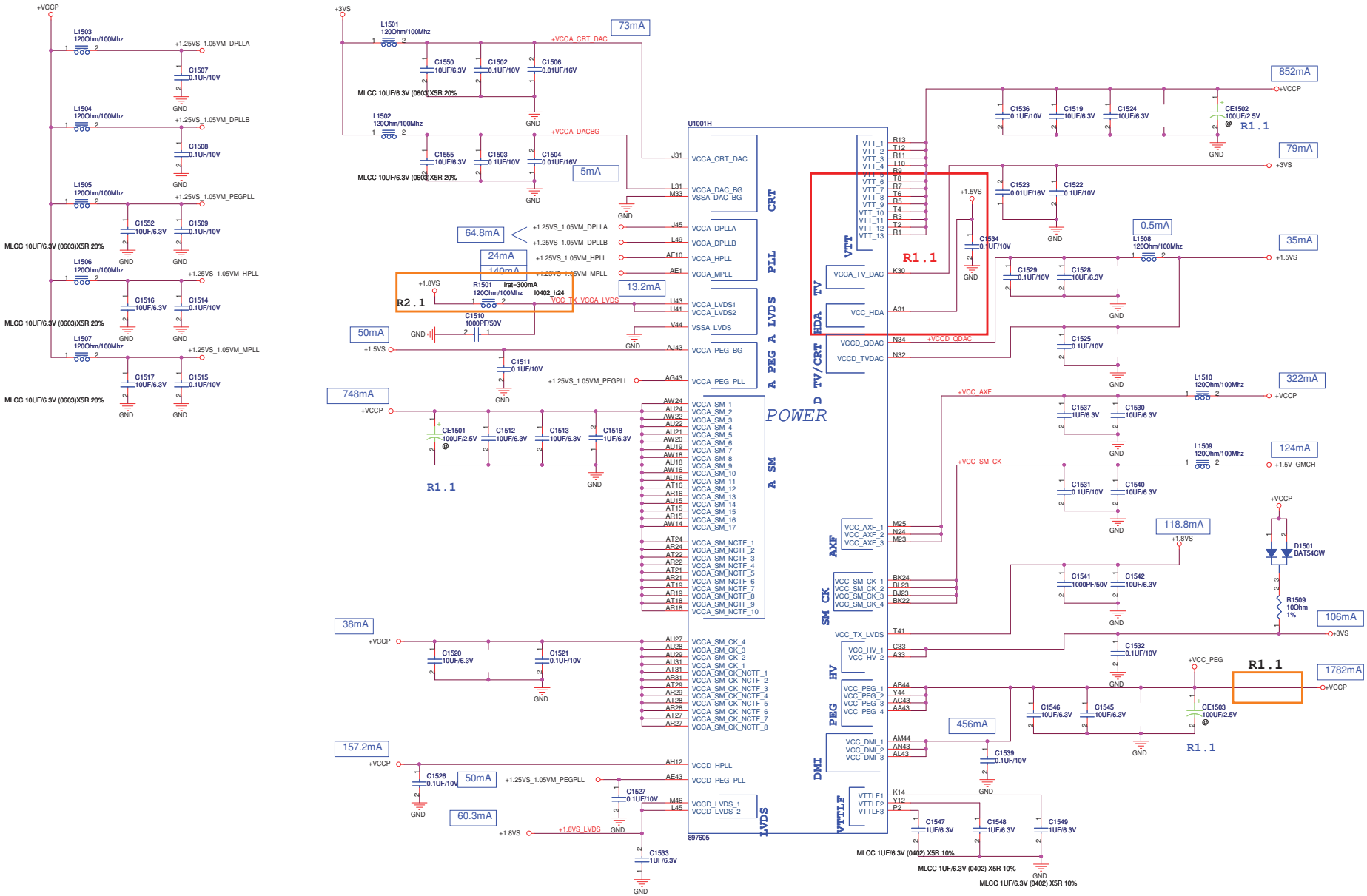
ASUSTeK COMPUTER INC.

Title : NB GS45 POWER

Engineer: Jack Hsu

Size	Project Name	Rev
C	UL50AT	2.0

Date: Friday, October 16, 2009 Sheet 14 of 97



<Variant Name>

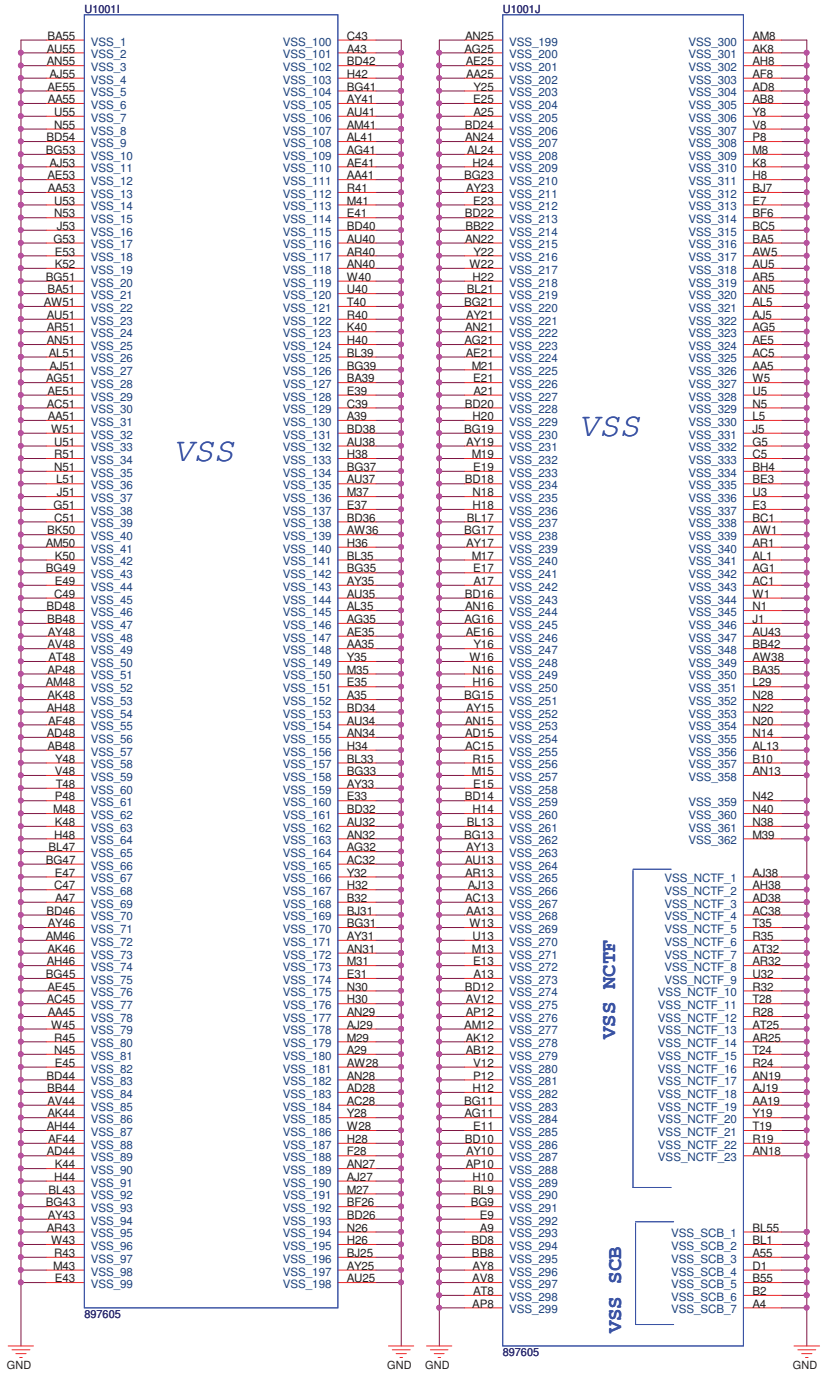
ASUSTeK COMPUTER INC.

Title : NB GS45 POWER

Engineer: Jack Hsu

Size	Project Name	Rev
C	UL50AT	2.0

Date: Friday, October 16, 2009 Sheet 15 of 97



<Variant Name>

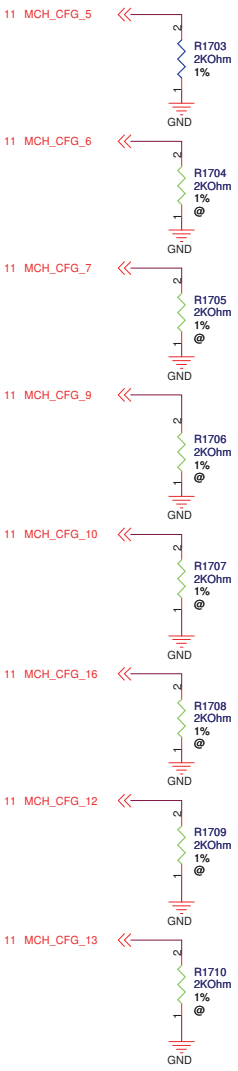
ASUSTeK COMPUTER INC.

Title : NB GS45 GND

Engineer: Jack Hsu

Size	Project Name	Rev
Custom	UL50AT	2.0

Date: Friday, October 16, 2009 Sheet 16 of 97



CFG5 : DMI STRAP
H = DMI X 4 (Default)
L = DMI X 2

CFG6 : ITPM Host Interface (Relate to SPI_MOSI)
H = ITPM Disable (Default)
L = ITPM enable(Can disable by SW)

CFG7 : Intel ME Crypto Strap
H = With confidentiality (Default)
L = Without confidentiality

CFG9 : PCIE Graphic Lane Reverse
H = Normal (Default)
L = Lanes Reverse

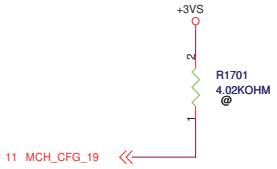
CFG10 : PCIE Loopback
H = Disable (Default)
L = Enable

CFG16 : FSB Dynamic ODT
H =Enable (Default)
L = Disable

CFG12 : ALL-Z Mode
H =Disable (Default)
L = Enable

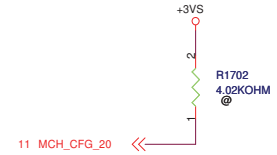
CFG13 : XOR Mode
H = Disable (Default)
L = Enable

CFG [13:12] : XOR/ALL-Z
00 = Reserved
01= XOR Mode Enabled
10= All-Z Mode Enabled
11= Normal Operation (Default)



CFG19 : DMI Lane Reversal

H =DMI Lane Reversal
L = Normal (Default)



CFG20 : SDVO/PCIE CONCURRENT MODE

L = Only Digital display port or PCIE is Operational (Default)
H = Digital display port and PCIE are operating simultaneously via the PEG port

<Variant Name>

ASUSTeK COMPUTER INC.

Title : NB GS45 STRAPPING

Engineer: Jack Hsu

Size	Project Name	Rev
Custom	UL50AT	2.0

Date: Friday, October 16, 2009 Sheet 17 of 97

<Variant Name>

Title :

ASUSTeK COMPUTER INC.

Engineer: Jack Hsu

Size	Project Name	Rev
C	UL50AT	2.0

Date: Friday, October 16, 2009 Sheet 18 of 97

<Variant Name>

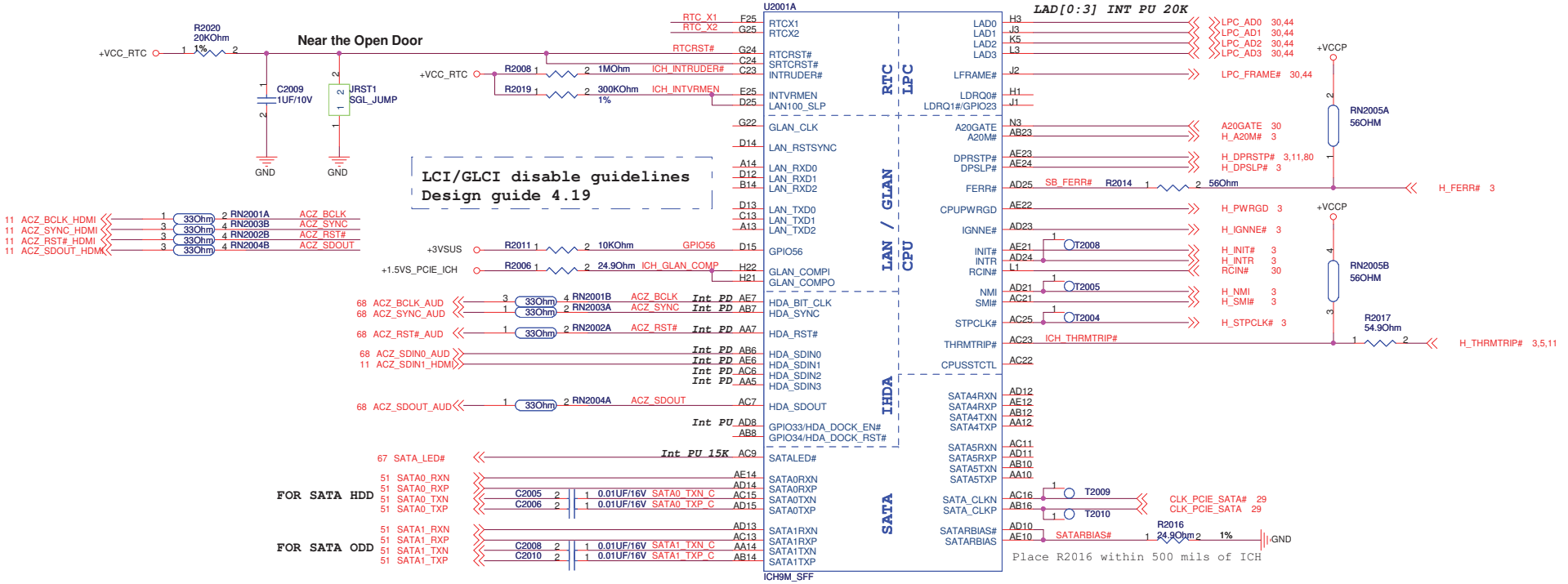
Title :

ASUSTeK COMPUTER INC.

Engineer: Jack Hsu

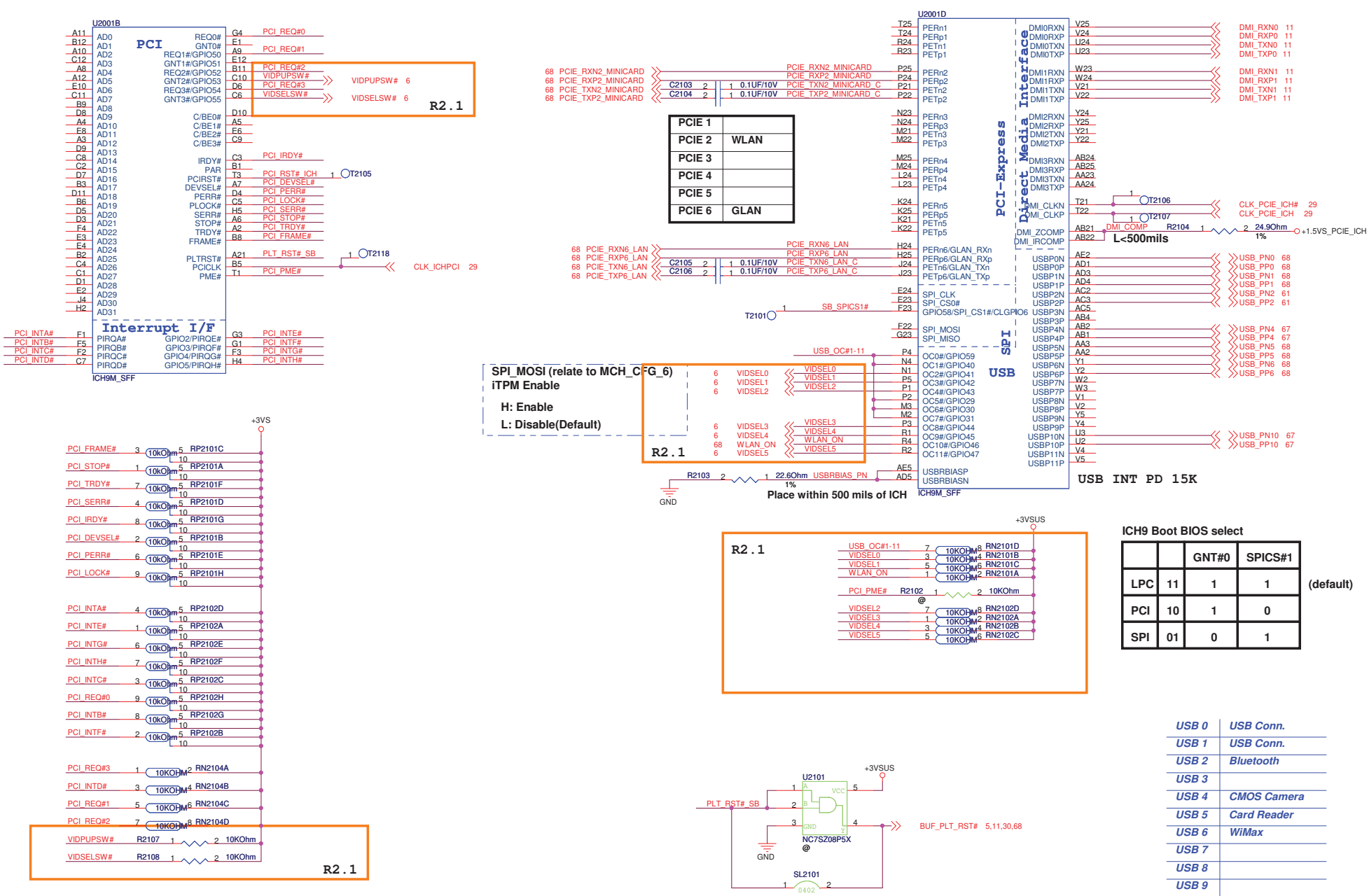
Size	Project Name	Rev
C	UL50AT	2.0

Date: Friday, October 16, 2009 Sheet 19 of 97



<Variant Name>

ASUSTeK COMPUTER INC.	Title : SB ICH9M (1)	
	Engineer: Jack Hsu	
Size: Custom	Project Name: UL50AT	Rev: 2.0
Date: Friday, October 16, 2009	Sheet 20 of 97	



PCIE 1	
PCIE 2	WLAN
PCIE 3	
PCIE 4	
PCIE 5	
PCIE 6	GLAN

ICH9 Boot BIOS select

		GNT#0	SPICS#1	
LPC	11	1	1	(default)
PCI	10	1	0	
SPI	01	0	1	

USB 0	USB Conn.
USB 1	USB Conn.
USB 2	Bluetooth
USB 3	
USB 4	CMOS Camera
USB 5	Card Reader
USB 6	WiMax
USB 7	
USB 8	
USB 9	
USB 10	USB Conn.
USB 11	

<Variant Name>

Title : SB ICH9M (2)

ASUSTeK COMPUTER INC. Engineer: Jack Hsu

Size	Project Name	Rev
Custom	UL50AT	2.0

Date: Friday, October 16, 2009 Sheet 21 of 97

SATA[X]GP unused need PU 10K to +3VS
(DG 4.2.6)

U2001C

SMB: SMBCLK, SMBDATA, LINKALERT#/GPIO60/CLGPIO2, SMLINK0, SMLINK1
SATA GPIO: GPIO21/SATA0GP, GPIO19/SATA1GP, GPIO36/SATA4GP, GPIO37/SATA5GP
Clocks: CLK14, CLK48
SYS GPIO / Power MGT: RI#, SUS_STAT#, SYS_RESET#, PMSYNC#/GPIO0, SMBALERT#/GPIO11, STPPCI#/GPIO15, STPCPU#/GPIO25, CLKRUN#/GPIO32, WAKE#, SERIRQ, THRM#, VRMPWRGD, TP11, SUSCLK, SLP_S3#, SLP_S4#, SLP_S5#, GPIO26/S4_STATE#, PWROK, DPRSLPVR/GPIO16, BATLOW#, PWRBTN#, LAN_RST#, RSMRST#, CK_PWRGD, CL_PWROK, SLP_M#
GPIO / Controller Link: GPIO1/TACH1, GPIO6, GPIO7, GPIO8, GPIO12/LAN_PHY_PWR_CTRL, GPIO13, GPIO17, GPIO18, GPIO20, GPIO22/SCLOCK, GPIO27, GPIO28, SATACLKREQ#/GPIO35, GPIO38/SLOAD, GPIO39/SDATAOUT0, GPIO48/SDATAOUT1, GPIO49, GPIO57/CLGPIO5, CL_CLK0, CL_CLK1, CL_DATA0, CL_DATA1, CL_VREF0, CL_VREF1, CL_RST0#, CL_ST1#
MISC: SPKR, MCH_SYNC#, TP3, TP8, TP9, TP10, GPIO24/MEM_LED, GPIO10/SUS_PWR_ACK, GPIO14/AC_PRESENT, GPIO9/WOL_EN

ICH9M_SFF

R1.1

SPKR
No Reboot Strap
Low = Default
High = No Reboot

CL1 not required if IAMT disable
DG 4.8

Follow DesignIP
Follow M51Va

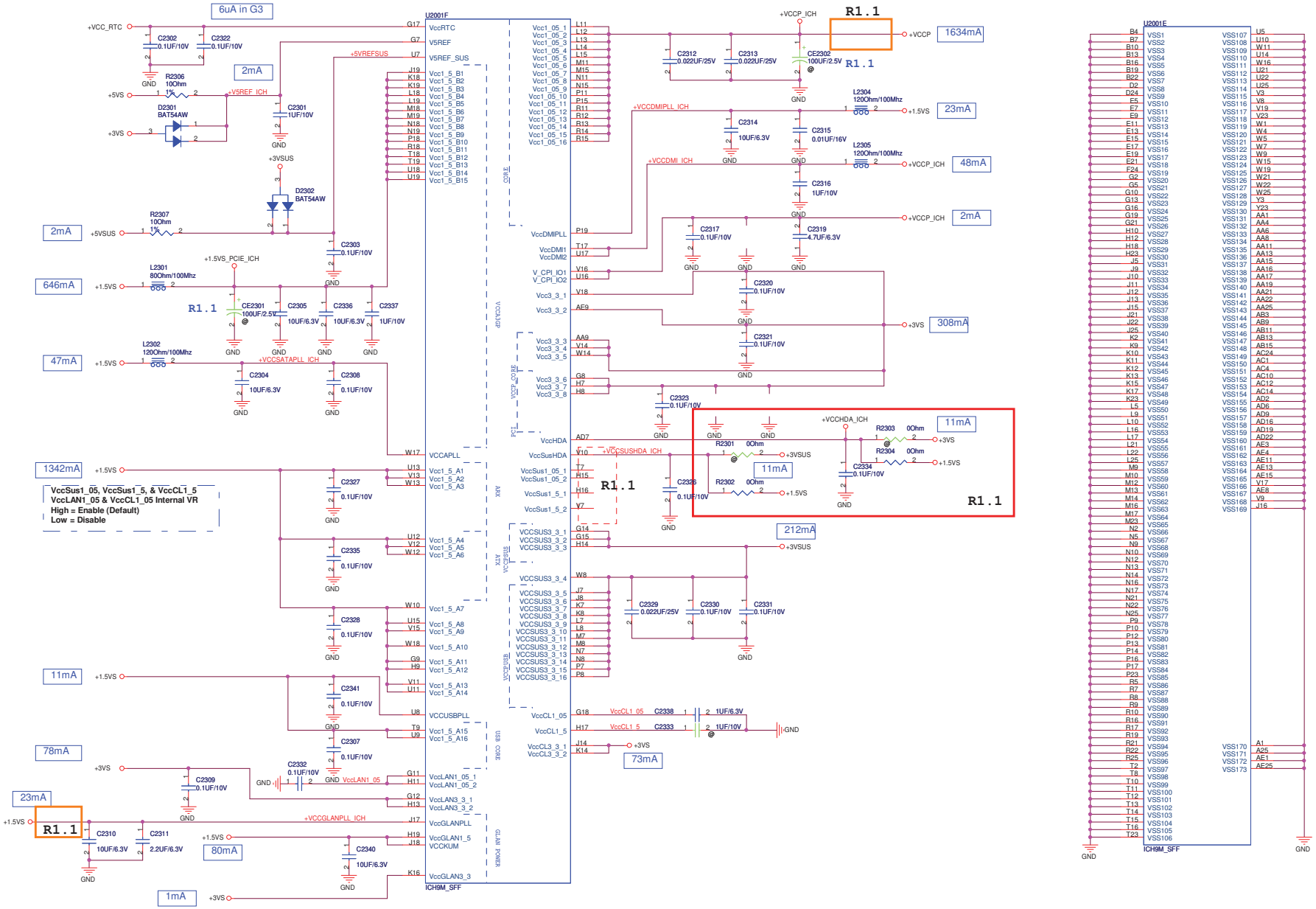
R2.0

PCB ID	GPIO38	GPIO39
UL50A	0	0
UL50V	0	1

CL_VREF0 routing rules
Width = 12 mils min
Spacing = 12 mils min
Break-out = 5 mils on 5 mils for 300 mils max

<Variant Name>

Title: SB ICH9M (3)
ASUSTeK COMPUTER INC.
Engineer: Jack Hsu
Size: Custom | Project Name: UL50AT | Rev: 2.0
Date: Friday, October 16, 2009 | Sheet 22 of 97



<Variant Name>

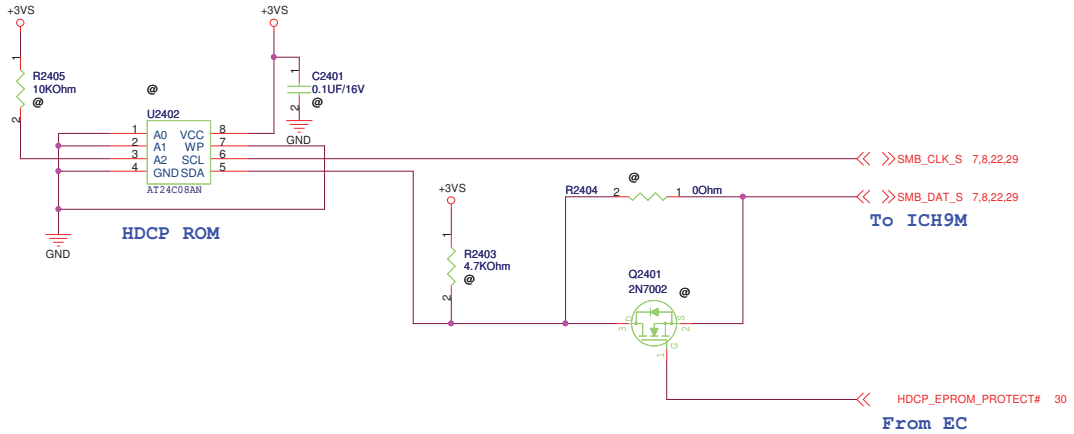
ASUSTeK COMPUTER INC.

Title : SB ICH9M (4)

Engineer: Jack Hsu

Size	Project Name	Rev
C	UL50AT	2.0

Date: Friday, October 16, 2009 Sheet 23 of 97



<Variant Name>

ASUSTeK COMPUTER INC.

Title : SB ICH9M (5)

Engineer: Jack Hsu

Size	Project Name	Rev
Custom	UL50AT	2.0

Date: Friday, October 16, 2009 Sheet 24 of 97

<Variant Name>

Title :

ASUSTeK COMPUTER INC.

Engineer: Jack Hsu

Size	Project Name	Rev
C	UL50AT	2.0

Date: Friday, October 16, 2009 Sheet 25 of 97

<Variant Name>

Title :

ASUSTeK COMPUTER INC.

Engineer: Jack Hsu

Size	Project Name	Rev
C	UL50AT	2.0

Date: Friday, October 16, 2009 Sheet 26 of 97

<Variant Name>

Title :

ASUSTeK COMPUTER INC.

Engineer: Jack Hsu

Size	Project Name	Rev
C	UL50AT	2.0

Date: Friday, October 16, 2009 Sheet 27 of 97

<Variant Name>

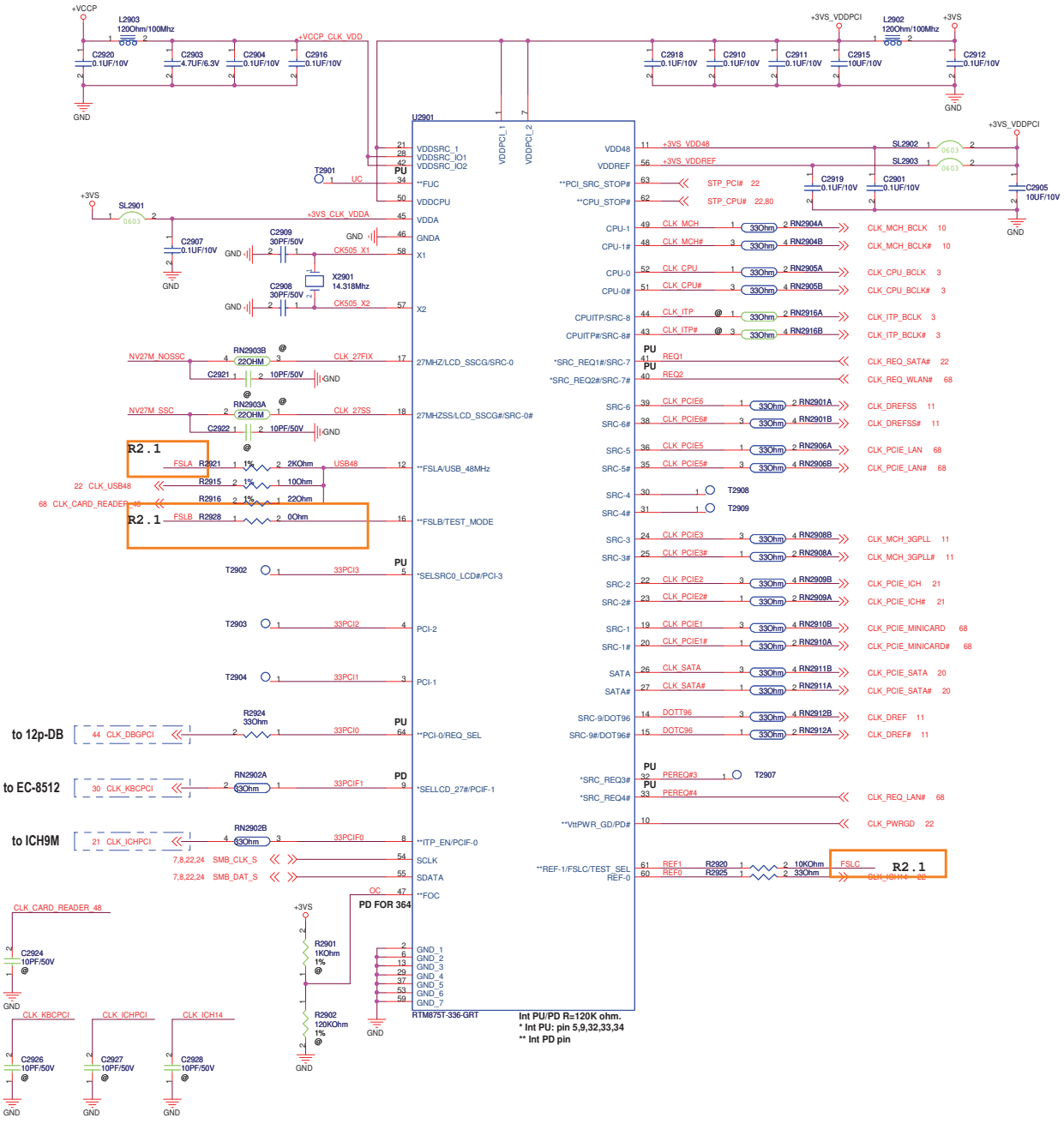
Title :

ASUSTeK COMPUTER INC.

Engineer: Jack Hsu

Size	Project Name	Rev
C	UL50AT	2.0

Date: Friday, October 16, 2009 Sheet 28 of 97



Latched Input Select

Pin5	Pin9	Pin14/15	Pin17/18
SELPCIEX0_LCD#/ PCI3 = 0 (low)	SELLCD_27#=0	PCIEX9	27FIX/SS
	SELLCD_27#=1	DOT96	LCD
SELPCIEX0_LCD#/ PCI3 = 1 (high)	SELLCD_27#=0	DOT96	27FIX/SS
	SELLCD_27#=1	DOT96	PCIEX0

Decide pin 43/44

0 = SRC CLK
1 = CPU_ITP CLK

(Pin8) ITP_EN — 33PCIF0 — 10KOHM — RN2913B

0 = LCDCLK
1 = PCIEX

Decide pin 17/18
96MHz (Non - SSC)
100MHz SSC

(Pin5) SELPCIE0_LCD# — 33PCI3 — RN2914A 10KOHM — +3VS

Decide pin 40/41

0 = PCIECLK
1 = PEREQ#

(Pin64) REQ_SEL# — 33PCI0 — 10KOHM — RN2914B — +3VS

Decide pin 17/18

SELLCD_27# = 0:
pin14/15=PCIEX_9L
pin17/18=27FIX/27SS

SELLCD_27# = 1:
pin14/15=DOT_96MHzL
pin17/18=LCD_SSCG/PCIe_L0

(Pin9) 33PCIF1 — 10KOHM — RN2913A

R2.1

3 CPU_BSEL0 — SL2904 — FSLA — R2918 — MCH_BSEL0 11
3 CPU_BSEL1 — R2927 — FSLB — R2919 — MCH_BSEL1 11
3 CPU_BSEL2 — SL2905 — FSLC — R2917 — MCH_BSEL2 11

30 FSB_SEL — Q2901A UM6K1N — Q2901B UM6K1N

BCLK	FSB	FSLC BSEL2	FSLB BSEL1	FSLA BSEL0
166	667	0	1	1
200	800	0	1	0
266	1066	0	0	0

<Variant Name>

ASUSTeK COMPUTER INC.

Title : RTM875T-336-GRT

Engineer: Jack Hsu

Size	Project Name	Rev
C	UL50AT	2.0

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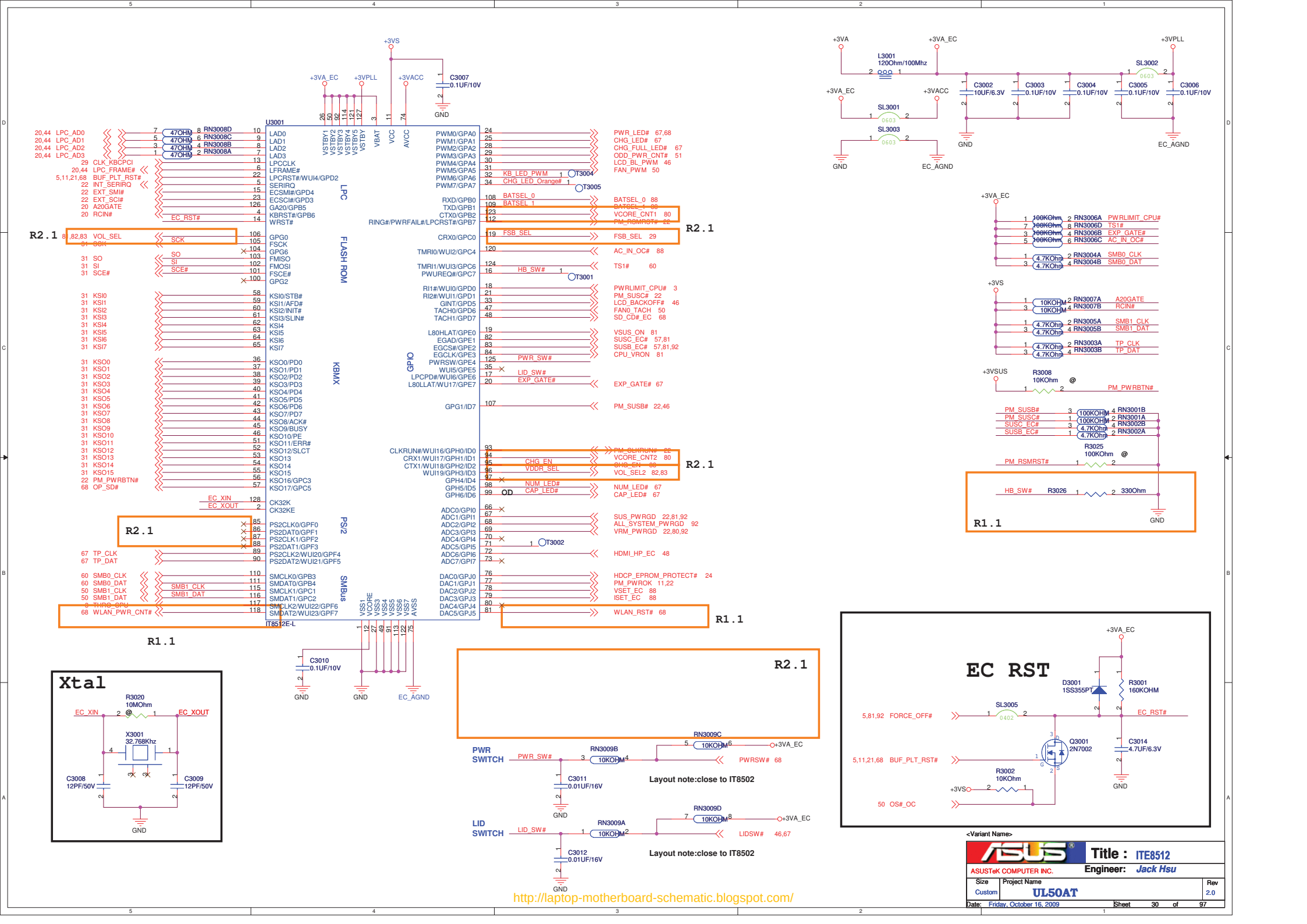
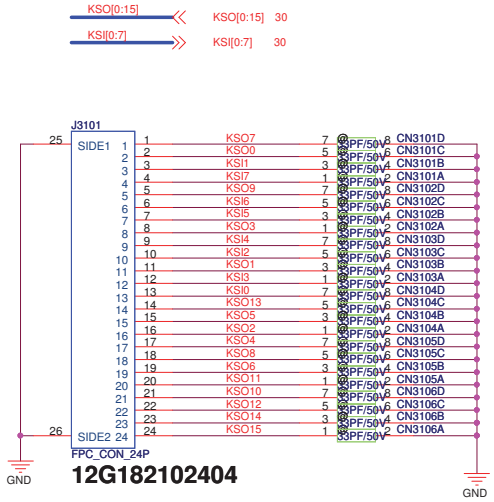


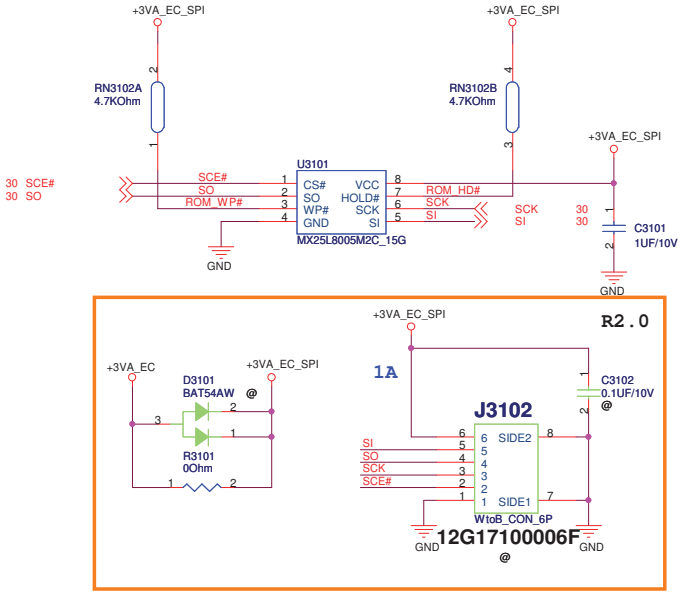
Title :	ITE8512
ASUSTeK COMPUTER INC.	Engineer: Jack Hsu
Size: Custom	Project Name: UL50AT
Rev: 2.0	
Date: Friday, October 16, 2009	Sheet 30 of 97

<Variant Name>

Internal Keyboard



SPI Flash ROM (8Mb)



<Variant Name>

ASUSTeK COMPUTER INC.	Title : KB & SPI ROM	
	Engineer: Jack Hsu	
Size: Custom	Project Name: UL50AT	Rev: 2.0
Date: Friday, October 16, 2009	Sheet 31 of 97	

<Variant Name>

ASUSTeK COMPUTER INC.	Title: <Title>	
	Engineer: Jack Hsu	
Size: C	Project Name: UL50AT	Rev: 2.0
Date: Friday, October 16, 2009	Sheet 32 of 97	

<Variant Name>

Title : <Title>

ASUSTeK COMPUTER INC.

Engineer: Jack Hsu

Size	Project Name	Rev
C	UL50AT	2.0

Date: Friday, October 16, 2009 Sheet 33 of 97

<Variant Name>

Title : <Title>

ASUSTeK COMPUTER INC.

Engineer: Jack Hsu

Size	Project Name	Rev
C	UL50AT	2.0

Date: Friday, October 16, 2009 Sheet 34 of 97

<Variant Name>

Title : <Title>

ASUSTeK COMPUTER INC.

Engineer: Jack Hsu

Size	Project Name	Rev
C	UL50AT	2.0

Date: Friday, October 16, 2009 Sheet 35 of 97

<Variant Name>

Title : <Title>

ASUSTeK COMPUTER INC.

Engineer: Jack Hsu

Size	Project Name	Rev
C	UL50AT	2.0

Date: Friday, October 16, 2009 Sheet 36 of 97

<Variant Name>

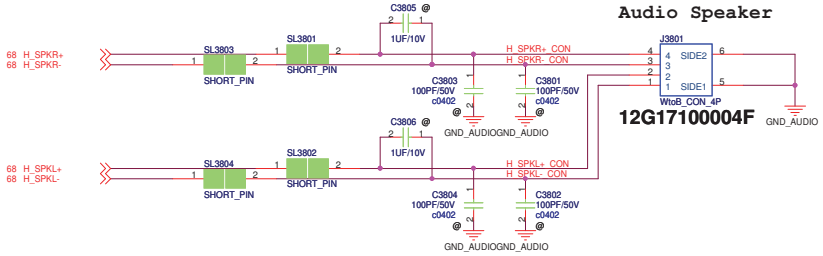
Title : <Title>

ASUSTeK COMPUTER INC.

Engineer: Jack Hsu

Size	Project Name	Rev
C	UL50AT	2.0

Date: Friday, October 16, 2009 Sheet 37 of 97



<Variant Name>

ASUSTeK COMPUTER INC.

Title : Internal Speaker

Engineer: Jack Hsu

Size	Project Name	Rev
C	UL50AT	2.0

Date: Friday, October 16, 2009 Sheet 38 of 97

<Variant Name>

Title : <Title>

ASUSTeK COMPUTER INC.

Engineer: Jack Hsu

Size	Project Name	Rev
C	UL50AT	2.0

Date: Friday, October 16, 2009 Sheet 39 of 97

<Variant Name>

Title :

ASUSTeK COMPUTER INC.

Engineer: Jack Hsu

Size	Project Name	Rev
C	UL50AT	2.0

Date: Friday, October 16, 2009 Sheet 40 of 97

<Variant Name>

Title :

ASUSTeK COMPUTER INC.

Engineer: Jack Hsu

Size	Project Name	Rev
C	UL50AT	2.0

Date: Friday, October 16, 2009 Sheet 41 of 97

<Variant Name>

Title : <Title>

ASUSTeK COMPUTER INC.

Engineer: Jack Hsu

Size	Project Name	Rev
C	UL50AT	2.0

Date: Friday, October 16, 2009 Sheet 42 of 97

<Variant Name>

Title : <Title>

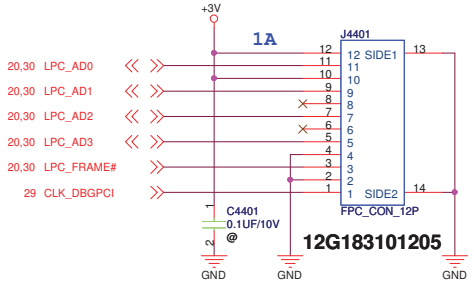
ASUSTeK COMPUTER INC.

Engineer: Jack Hsu

Size	Project Name	Rev
C	UL50AT	2.0

Date: Friday, October 16, 2009 Sheet 43 of 97

LPC DEBUG PORT



<Variant Name>

ASUSTeK COMPUTER INC.

Title : DEBUG PORT

Engineer: Jack Hsu

Size	Project Name	Rev
Custom	UL50AT	2.0

Date: Friday, October 16, 2009 Sheet 44 of 97

<Variant Name>

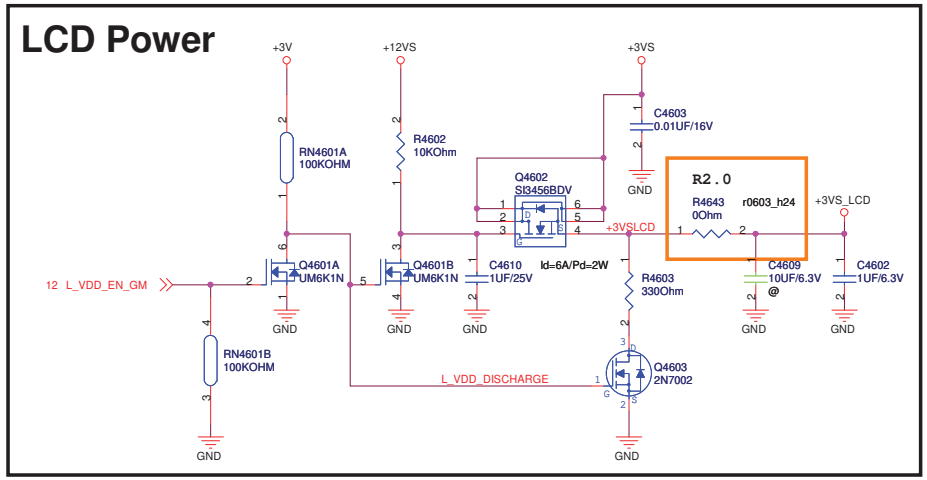
Title : <Title>

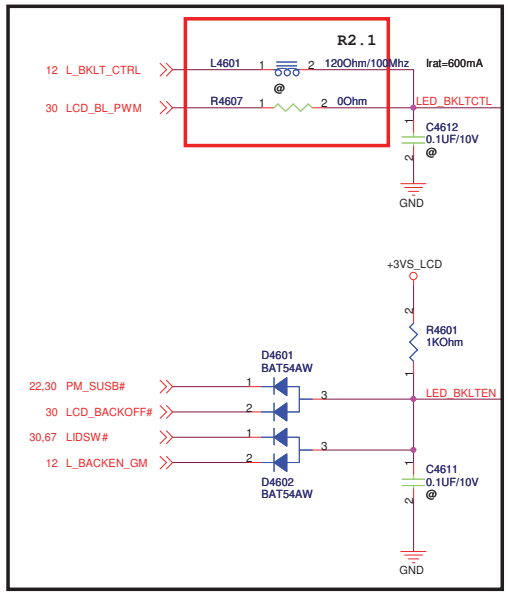
ASUSTeK COMPUTER INC.

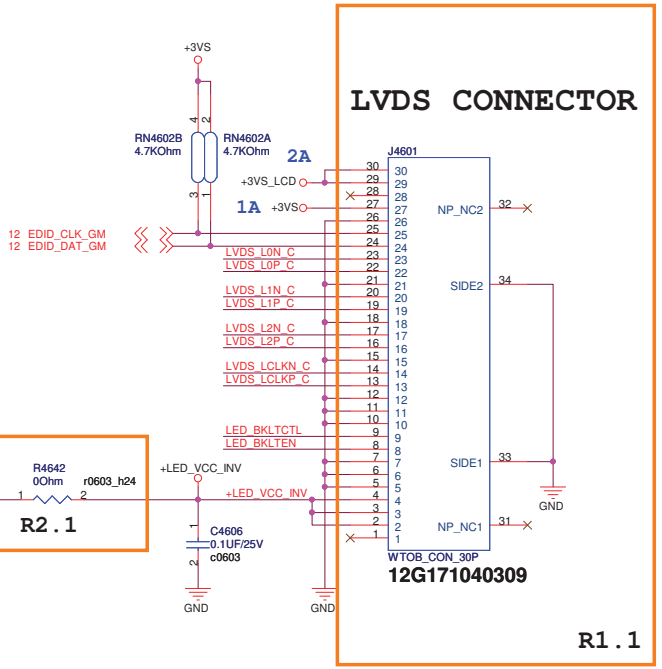
Engineer: Jack Hsu

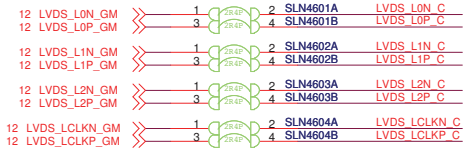
Size	Project Name	Rev
C	UL50AT	2.0

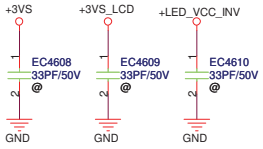
Date: Friday, October 16, 2009 Sheet 45 of 97











<variant_name>

ASUSTeK COMPUTER INC.	Title : LVDS CONNECTOR	
	Engineer: Jack Hsu	
Size: Custom	Project Name: UL50AT	Rev: 2.0
Date: Friday, October 16, 2009	Sheet 46 of 97	

<Variant Name>

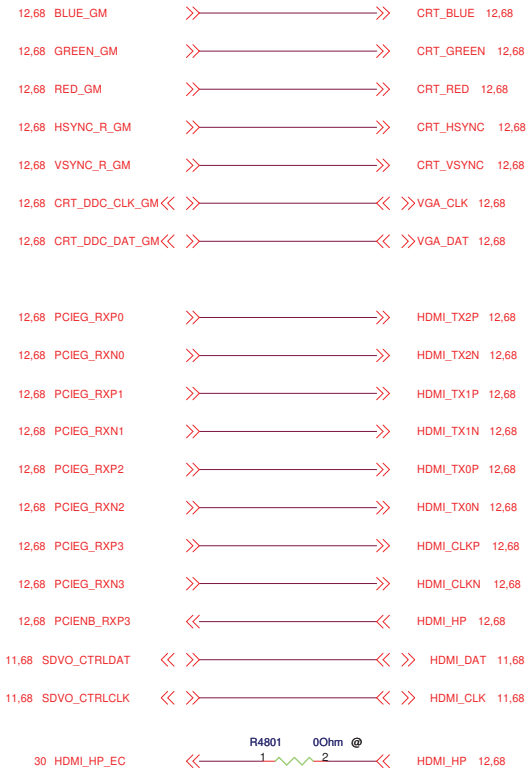
Title : <Title>

ASUSTeK COMPUTER INC.

Engineer: Jack Hsu

Size	Project Name	Rev
C	UL50AT	2.0

Date: Friday, October 16, 2009 Sheet 47 of 97



<Variant Name>

ASUSTeK COMPUTER INC.

Title : Hybrid Switch

Engineer: Jack Hsu

Size	Project Name	Rev
Custom	UL50AT	2.0

Date: Friday, October 16, 2009 Sheet 48 of 97

<Variant Name>

Title : HDMI LEVEL SHIFT

ASUSTeK COMPUTER INC.

Engineer: Jack Hsu

Size	Project Name	Rev
C	UL50AT	2.0

Date: Friday, October 16, 2009 Sheet 49 of 97

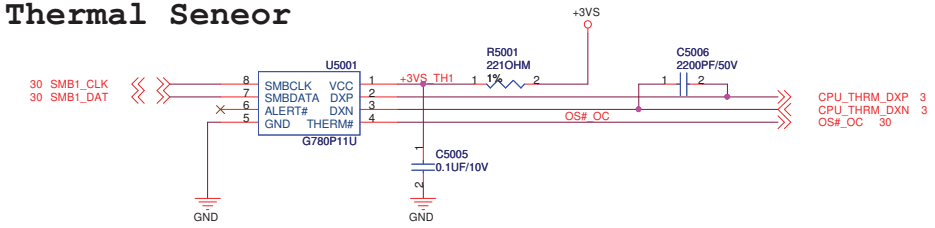
1nd: 06G023096010 G780P11U SOP-8
2nd: 06G023026012 MAX6657YMS+ SOP-8

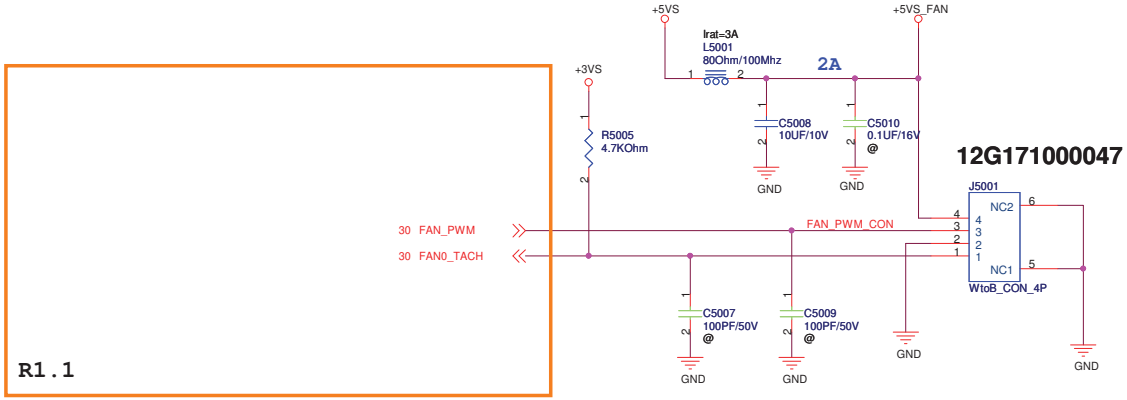
Route CPU_THRM_DA , CPU_THRM_DC and MEM_THERM_DA , MEM_THERM_DC on the same layer

----------OTHER SIGNALS
10 mils
==========GND
10 mils
==========H_THERMDA(10 mils)
10 mils
==========H_THERMDC(10 mils)
10 mils
==========GND
10 mils
----------OTHER SIGNALS

Avoid FSB,Power

Thermal Seneor

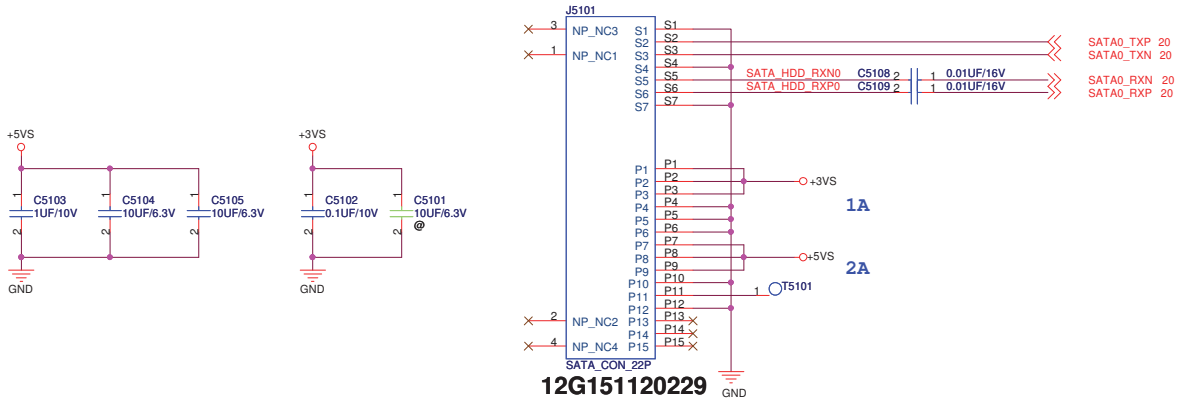




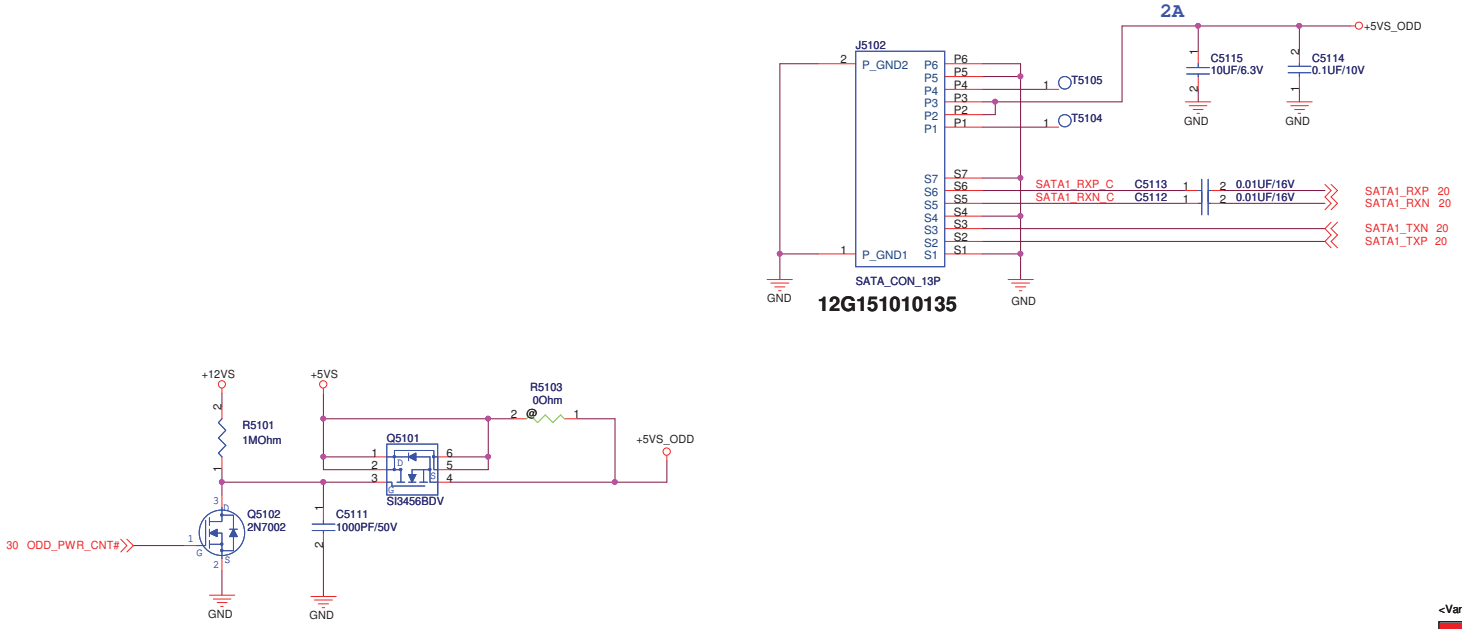
<Variant Name>

ASUSTeK COMPUTER INC.	Title : THERMAL & FAN	
	Engineer: Jack Hsu	
Size: Custom	Project Name: UL50AT	Rev: 2.0
Date: Friday, October 16, 2009	Sheet 50 of 97	

SATA HDD



SATA ODD



<Variant Name>

ASUSTeK COMPUTER INC.	Title : SATA HDD & ODD	
	Engineer: Jack Hsu	
Size: Custom	Project Name: UL50AT	Rev: 2.0
Date: Friday, October 16, 2009	Sheet 51 of 97	

<Variant Name>

Title : <Title>

ASUSTeK COMPUTER INC.

Engineer: Jack Hsu

Size	Project Name	Rev
C	UL50AT	2.0

Date: Friday, October 16, 2009 Sheet 52 of 97

<Variant Name>

Title : <Title>

ASUSTeK COMPUTER INC.

Engineer: Jack Hsu

Size	Project Name	Rev
C	UL50AT	2.0

Date: Friday, October 16, 2009 Sheet 53 of 97

<Variant Name>

Title : <Title>

ASUSTeK COMPUTER INC.

Engineer: Jack Hsu

Size	Project Name	Rev
C	UL50AT	2.0

Date: Friday, October 16, 2009 Sheet 54 of 97

<Variant Name>

Title : <Title>

ASUSTeK COMPUTER INC.

Engineer: Jack Hsu

Size	Project Name	Rev
C	UL50AT	2.0

Date: Friday, October 16, 2009 Sheet 55 of 97

<Variant Name>

Title : LID

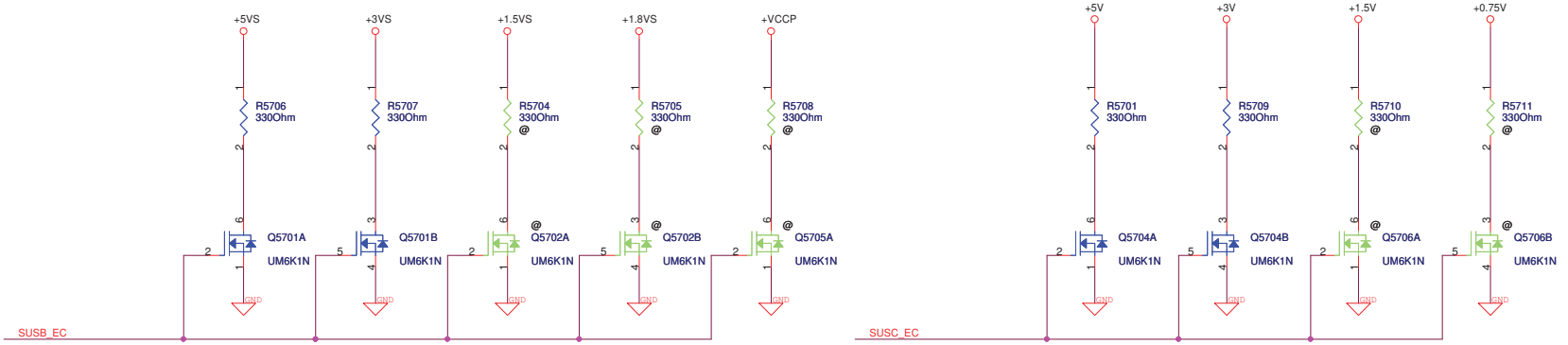
ASUSTeK COMPUTER INC.

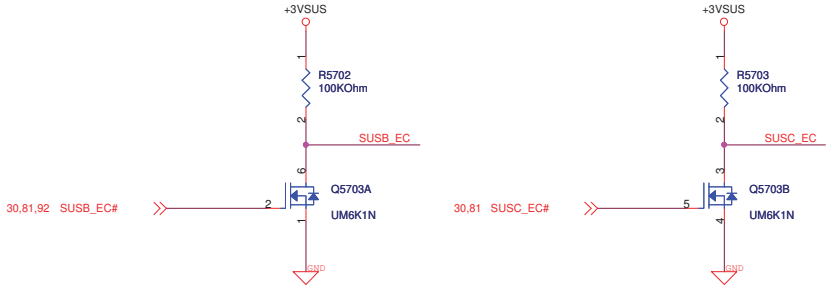
Engineer: Jack Hsu

Size	Project Name	Rev
Custom	UL50AT	2.0

Date: Friday, October 16, 2009 Sheet 56 of 97

Discharge Circuit





<Variant Name>

ASUSTeK COMPUTER INC.	Title DISCHARGE CIRCUIT	
	Engineer: Jack Hsu	
Size: Custom	Project Name: UL50AT	Rev: 2.0
Date: Friday, October 16, 2009	Sheet 57 of 97	

<Variant Name>

Title : <Title>

ASUSTeK COMPUTER INC.

Engineer: Jack Hsu

Size	Project Name	Rev
C	UL50AT	2.0

Date: Friday, October 16, 2009 Sheet 58 of 97

<Variant Name>

Title :

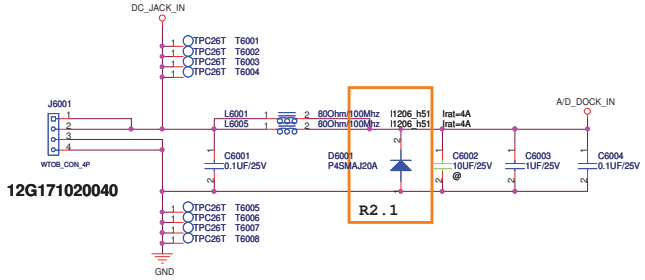
ASUSTeK COMPUTER INC.

Engineer: Jack Hsu

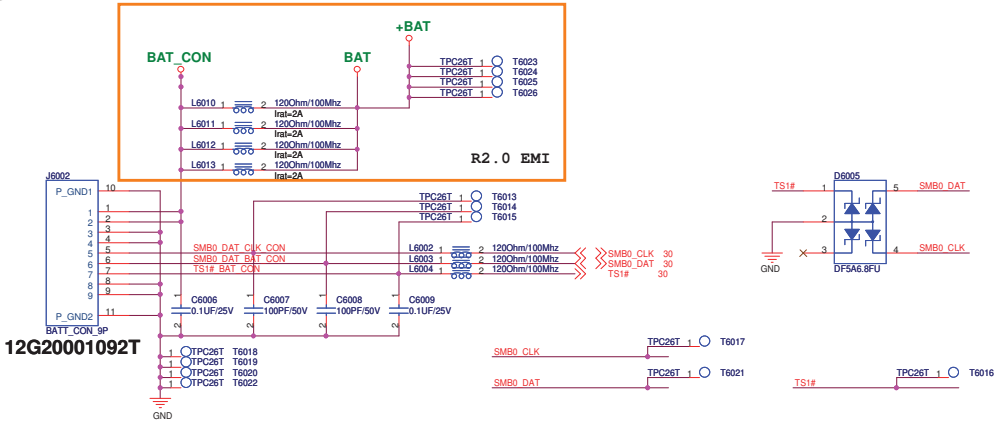
Size	Project Name	Rev
C	UL50AT	2.0

Date: Friday, October 16, 2009 Sheet 59 of 97

DC-IN

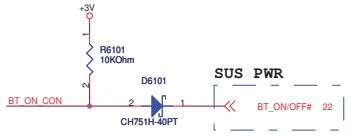


Battery Connector



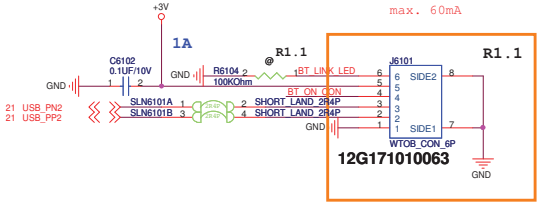
<Variant Name>

ASUSTeK COMPUTER INC.	Title : DC IN & BAT IN	
	Engineer: Jack Hsu	
Size: C	Project Name: UL50AT	Rev: 2.0
Date: Friday, October 16, 2009	Sheet 60 of 97	



Bluetooth Connector

max. 60mA



<Variant Name>

ASUSTeK COMPUTER INC.

Title : BlueTooth

Engineer: Jack Hsu

Size	Project Name	Rev
C	UL50AT	2.0

Date: Friday, October 16, 2009 Sheet 61 of 97

<Variant Name>

Title : <Title>

ASUSTeK COMPUTER INC.

Engineer: Jack Hsu

Size	Project Name	Rev
C	UL50AT	2.0

Date: Friday, October 16, 2009 Sheet 62 of 97

<Variant Name>

Title : <Title>

ASUSTeK COMPUTER INC.

Engineer: Jack Hsu

Size	Project Name	Rev
C	UL50AT	2.0

Date: Friday, October 16, 2009 Sheet 63 of 97

<Variant Name>

Title : <Title>

ASUSTeK COMPUTER INC.

Engineer: Jack Hsu

Size	Project Name	Rev
C	UL50AT	2.0

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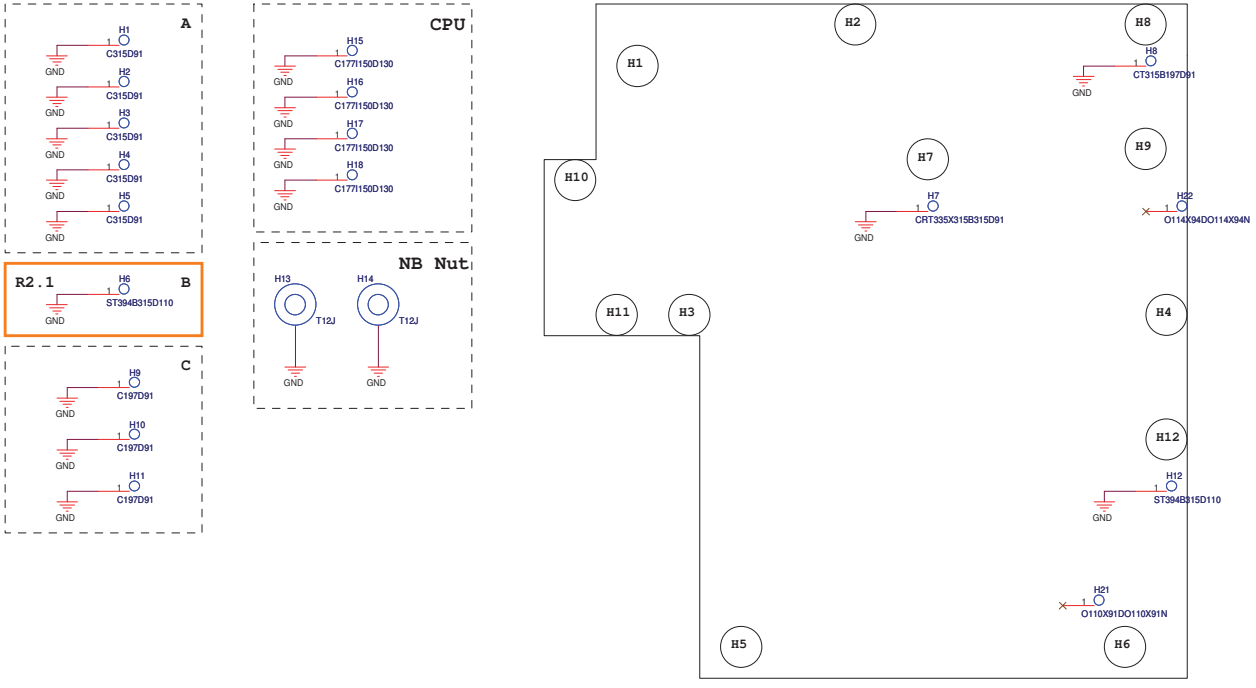
Screw Hole & SMT Nut



<Variant Name>

ASUSTeK COMPUTER INC.	Title : SCREW HOLE & NUT	
	Engineer: Jack Hsu	
Size: C	Project Name: UL50AT	Rev: 2.0
Date: Friday, October 16, 2009	Sheet 65 of 97	

<Variant Name>

Title :

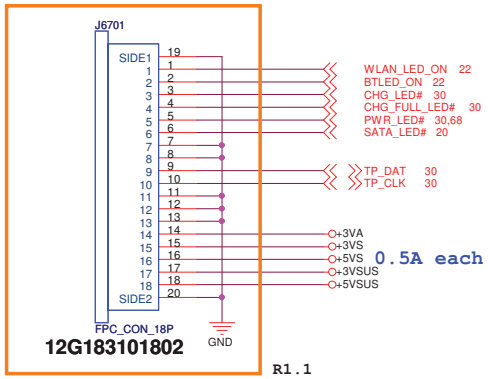
ASUSTeK COMPUTER INC.

Engineer: Jack Hsu

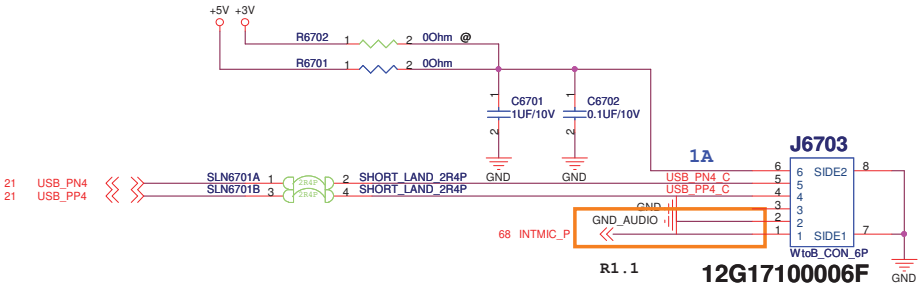
Size	Project Name	Rev
C	UL50AT	2.0

Date: Friday, October 16, 2009 Sheet 66 of 97

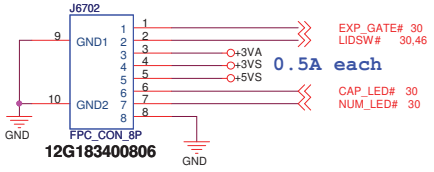
Touch Pad / LED Board

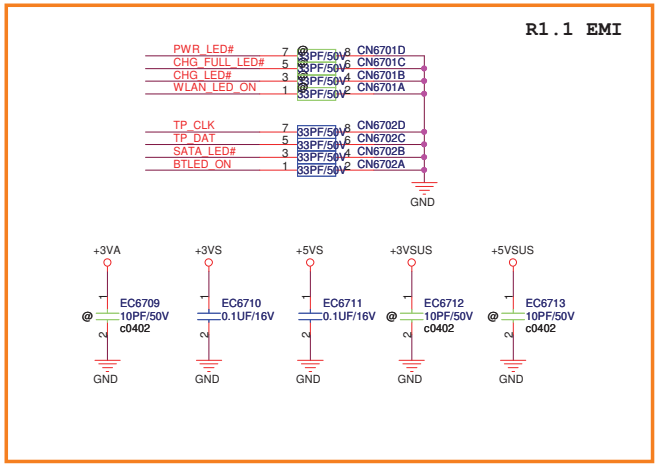


Camera Module

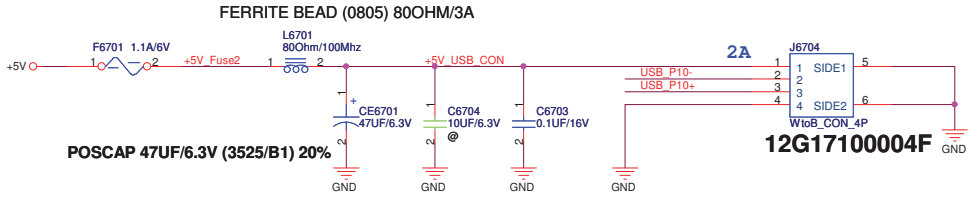


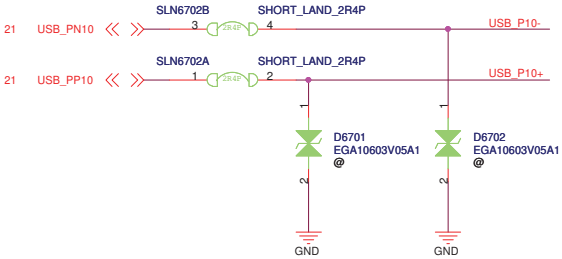
Function Board

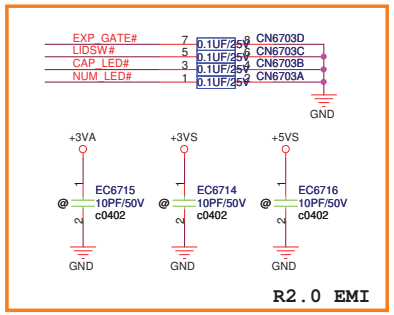


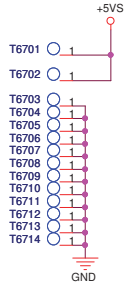


FLY USB Cable









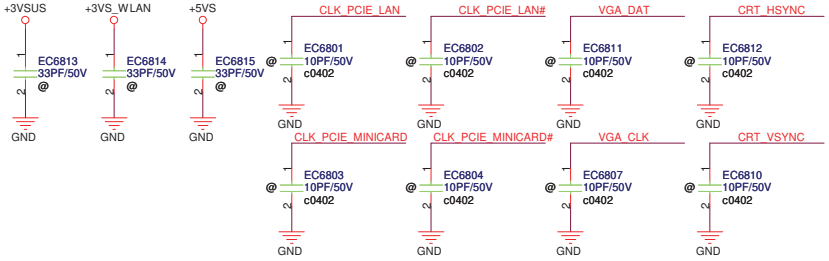
<Variant Name>

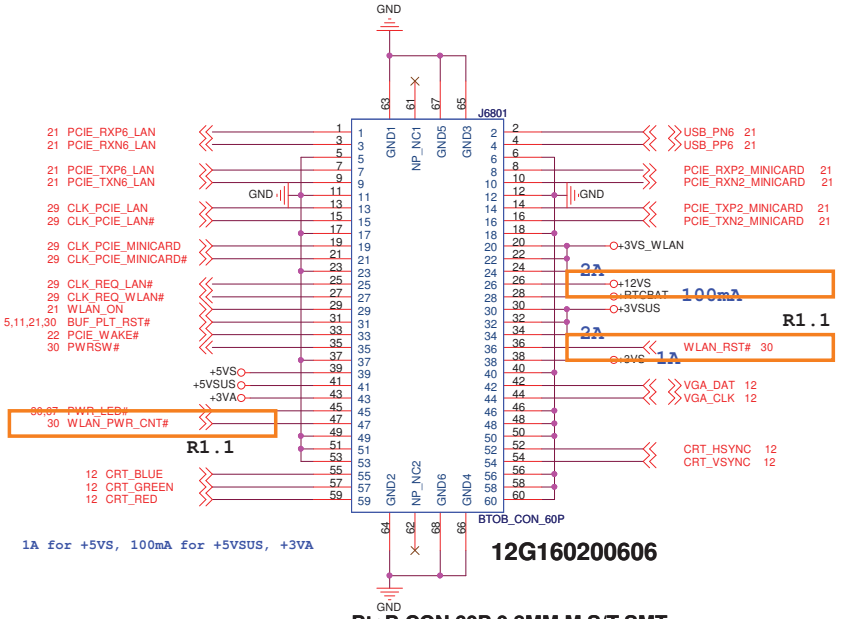
ASUSTeK COMPUTER INC.	Title : SUB BOARD	
	Engineer: Jack Hsu	
Size: Custom	Project Name: UL50AT	Rev: 2.0
Date: Friday, October 16, 2009	Sheet 67 of 97	

IO BOARD - 02

LAN IC
RJ45
CRT
RTC Conn.
MiniCard

WLAN Power Source Selection





1A for +5VS, 100mA for +5VSUS, +3VA

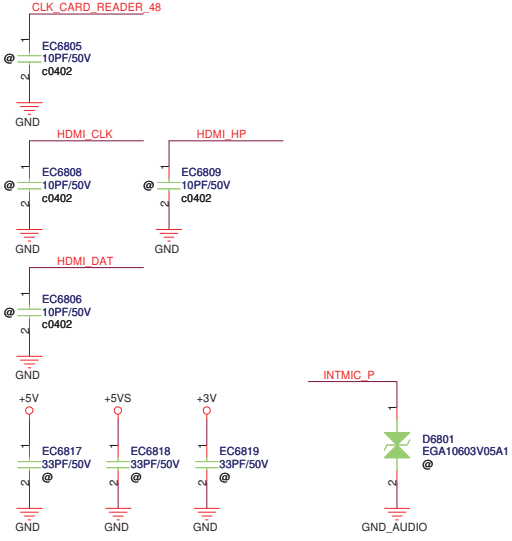
12G160200606

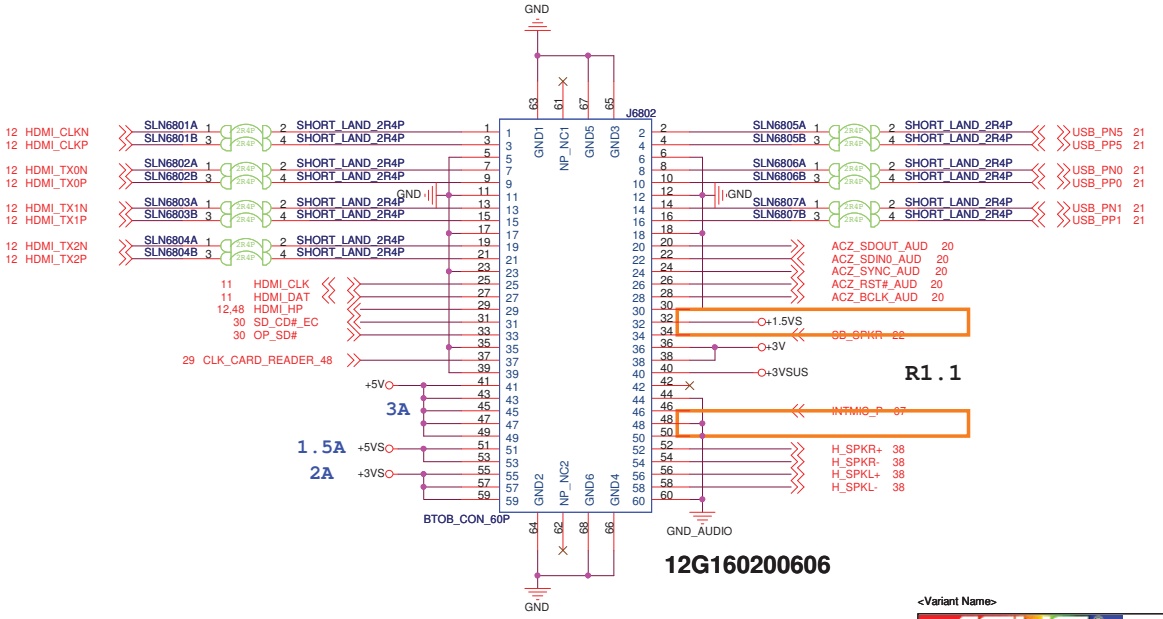
BtoB CON 60P,0.8MM,M,S/T,SMT

USB 0	USB Conn.
USB 1	USB Conn.
USB 2	Bluetooth
USB 3	
USB 4	CMOS Camera
USB 5	Card Reader
USB 6	WiMax
USB 7	
USB 8	
USB 9	
USB 10	USB Conn.
USB 11	

IO BOARD - 01

HDMI Conn.
USB Conn.x2
MIC-IN Conn.
Head Phone Conn.
Audio IC
Card Reader IC
Card Reader Conn.





12G160200606

BtoB CON 60P,0.8MM,M,S/T,SMT

<Variant Name>

ASUSTeK COMPUTER INC.	Title : B TO B CONNECTOR		
	Engineer: Jack Hsu		
Size: Custom	Project Name: UL50AT		Rev: 2.0
Date: Friday, October 16, 2009	Sheet 68 of 97		

<Variant Name>

Title : <Title>

ASUSTeK COMPUTER INC.

Engineer: Jack Hsu

Size	Project Name	Rev
C	UL50AT	2.0

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ASUSTeK COMPUTER INC.	Title : N10M-GE1 (1)	
	Engineer: Alan Chen	
Size: C	Project Name: <Variant Name> UL50AT	Rev: 2.0
Date: Friday, October 16, 2009	Sheet 70 of 97	

ASUSTeK COMPUTER INC.	Title : N10M-GE1 (2)	
	Engineer: Alan Chen	
Size: C	Project Name: UL50AT	Rev: 2.0
Date: Friday, October 16, 2009	Sheet 71 of 97	

ASUSTeK Computer Inc.	Title : N10M-GE1 (3)	
	Engineer: Alan Chen	
Size: C	Project Name: UL50AT	Rev: 2.0
Date: Friday, October 16, 2009	Sheet 72 of 97	

ASUSTeK COMPUTER INC.	Title : N10M-GE1 (4)		
	Engineer: Alan Chen		
Size: C	Project Name: UL50AT		Rev: 2.0
Date: Friday, October 16, 2009	Sheet 73 of 97		

ASUSTeK COMPUTER INC.	Title : N10M-GE1 (5)	
	Engineer: Alan Chen	
Size: C	Project Name: UL50AT	Rev: 2.0
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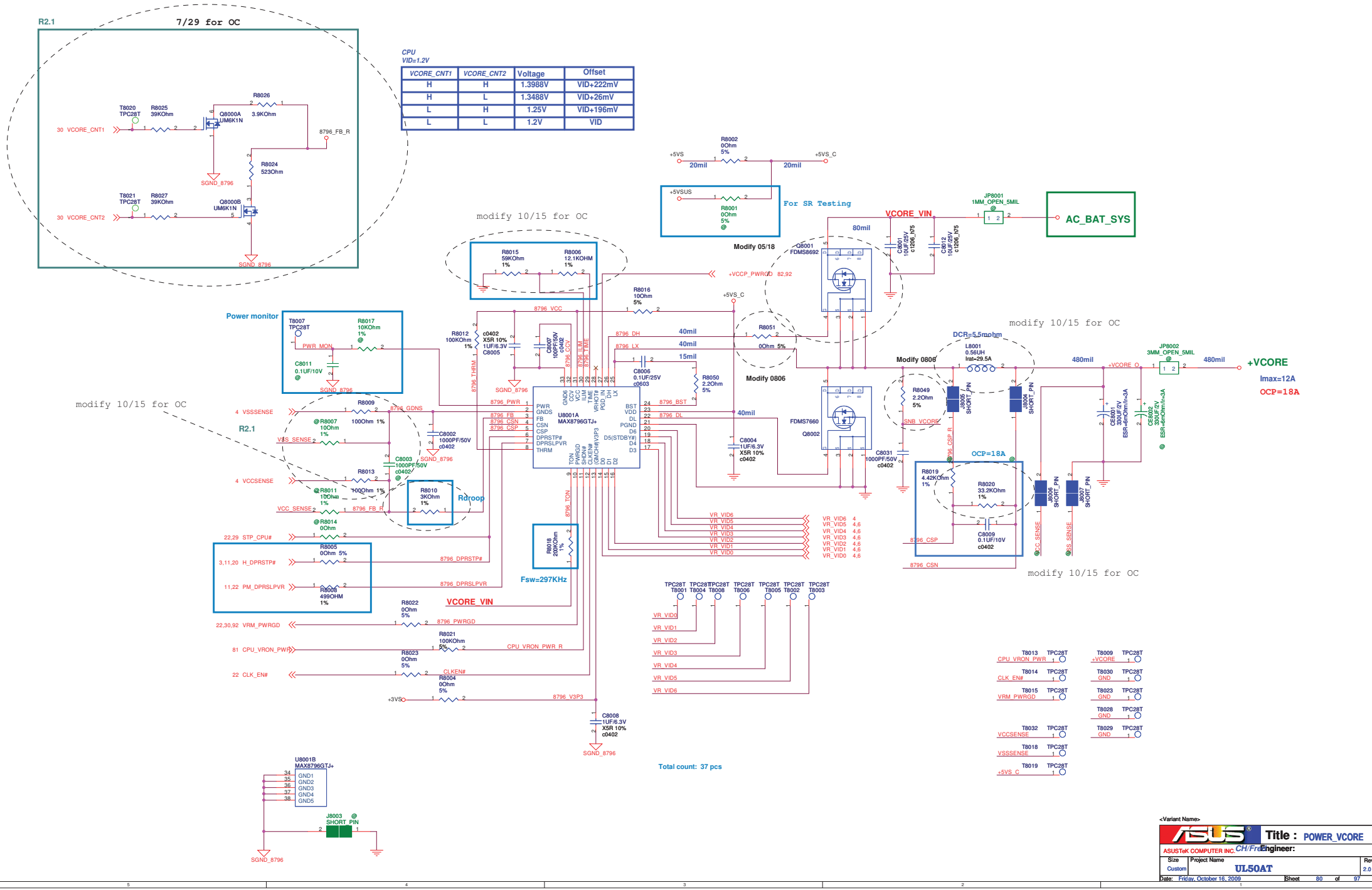
Variant Name:	Title : N10M-GE1 (6)	
ASUSTeK COMPUTER INC.	Engineer: Alan Chen	
Size: C	Project Name: UL50AT	Rev: 2.0
Date: Friday, October 16, 2009	Sheet 75 of 97	

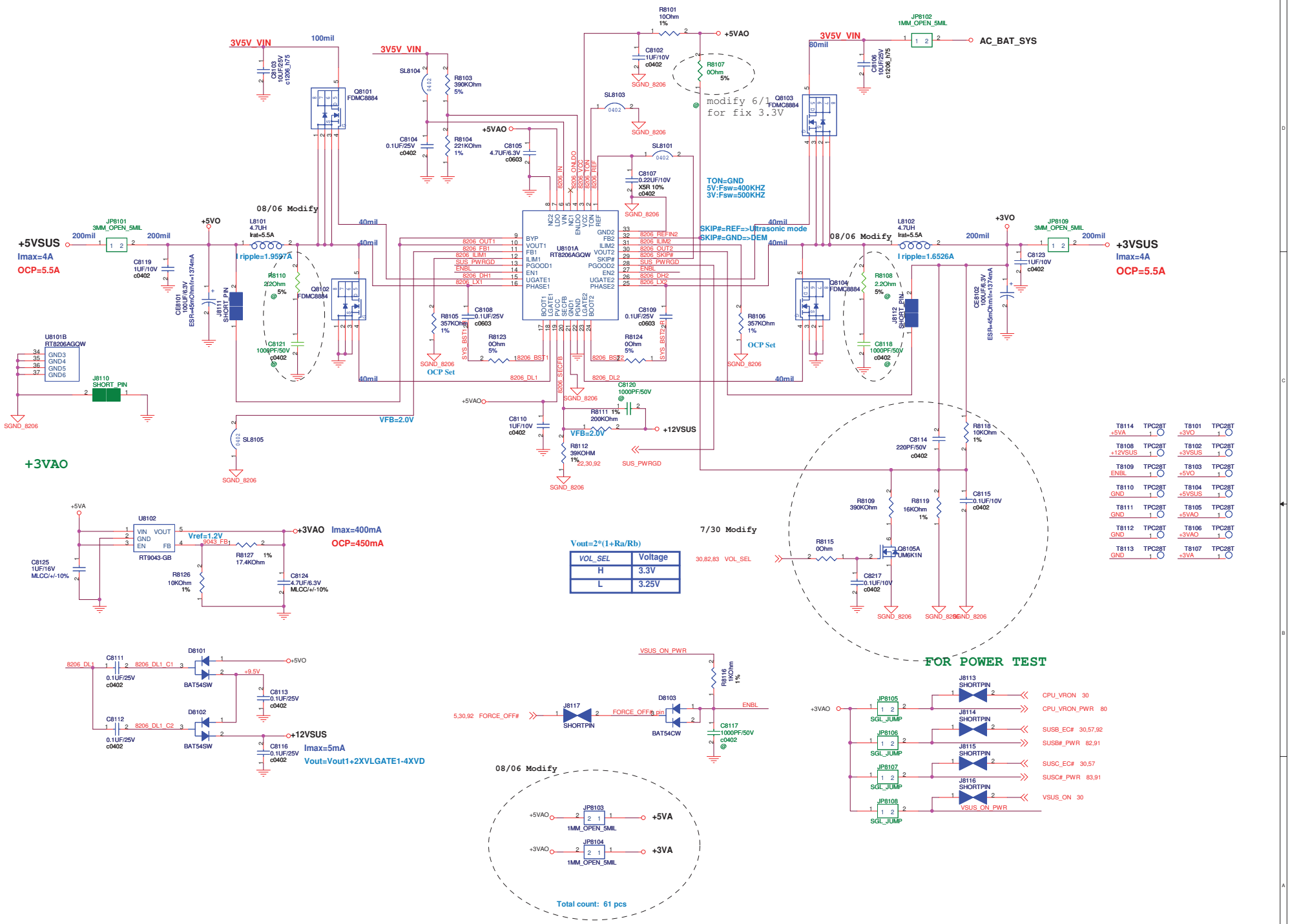
ASUSTeK COMPUTER INC.	Title : VGA Power Sequence	
	Engineer: Alan Chen	
Size: C	Project Name: UL50AT	Rev: 2.0
Date: Friday, October 16, 2009	Sheet 76 of 97	

ASUSTeK COMPUTER INC.	Title: <Title>	
	Engineer: Alan Chen	
Size: C	Project Name: UL50AT <Variant Name>	Rev: 2.0
Date: Friday, October 16, 2009	Sheet 77 of 97	

ASUSTeK COMPUTER INC.	Title: <Title>	
	Engineer: Alan Chen	
Size: C	Project Name: UL50AT	Rev: 2.0
Date: Friday, October 16, 2009	Sheet 78 of 97	

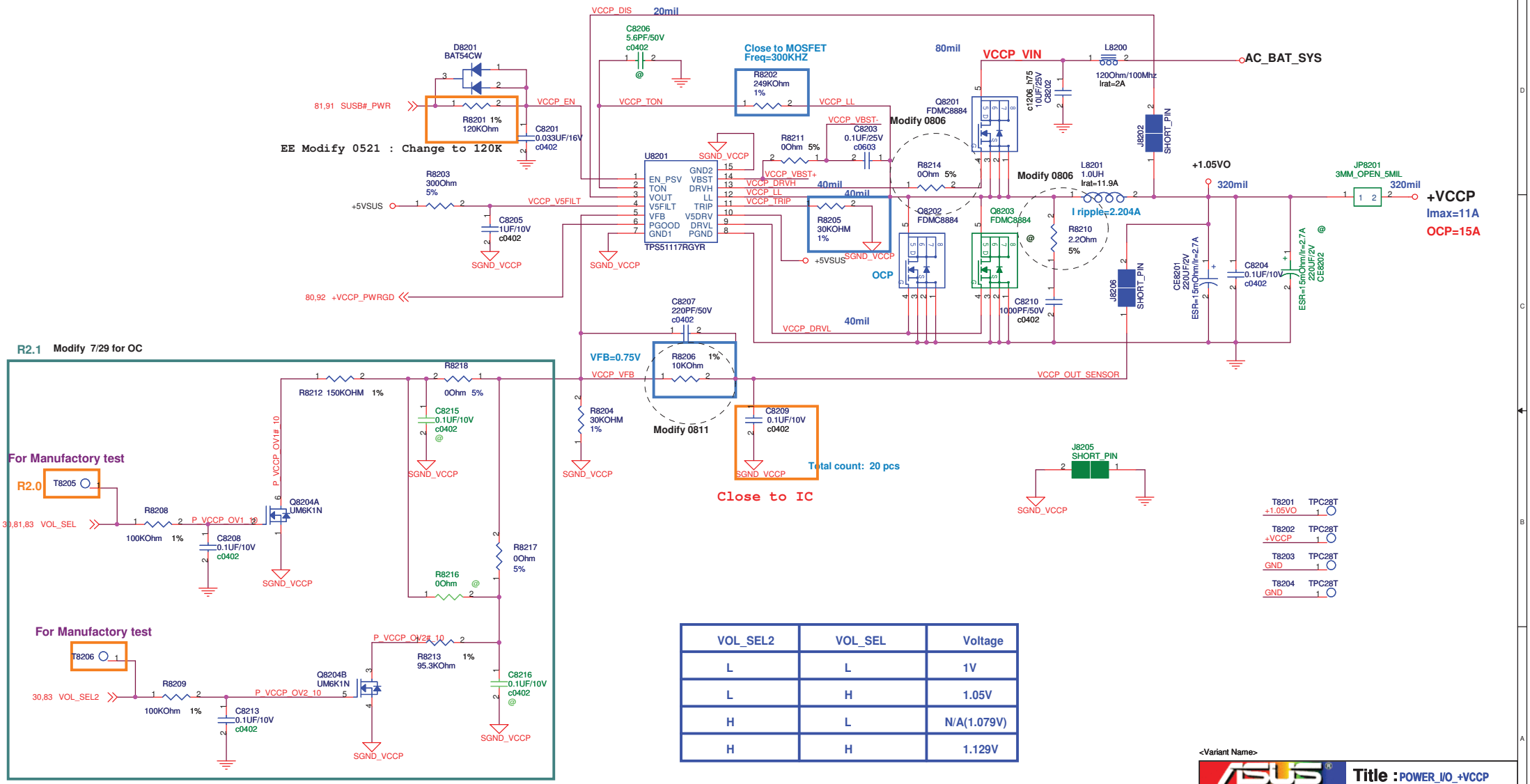
ASUSTeK COMPUTER INC.	Title: <Title>	
	Engineer: Alan Chen	
Size: C	Project Name: UL50AT	Rev: 2.0
Date: Friday, October 16, 2009	Sheet 79 of 97	





<variant_name>

ASUSTeK COMPUTER INC.	Title : POWER_SYSTEM	
CHFred	Engineer:	
Size: Custom	Project Name: UL50AT	Rev: 2.0
Date: Friday, October 16, 2009	Sheet 81 of 97	



VOL_SEL2	VOL_SEL	Voltage
L	L	1V
L	H	1.05V
H	L	N/A(1.079V)
H	H	1.129V

<Variant Name>

Title : POWER_I/O_+VCCP

ASUSTeK COMPUTER INC.

Engineer: CH/Fred

Size	Project Name	Rev
Custom	UL50AT	2.0

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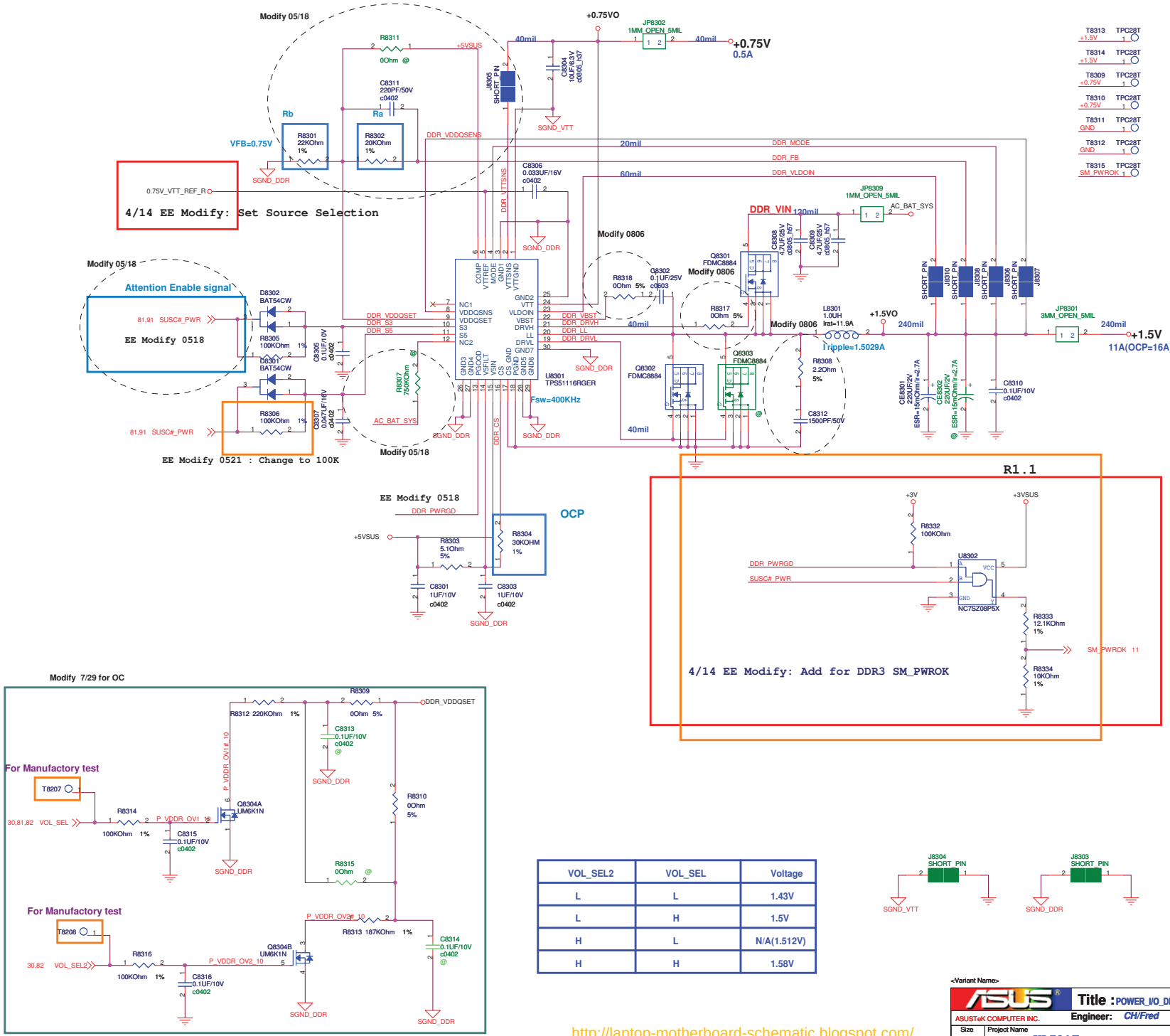

VOL_SEL2	VOL_SEL	Voltage
L	L	1.43V
L	H	1.5V
H	L	N/A(1.512V)
H	H	1.58V

<Variant Name>

ASUSTeK COMPUTER INC.

Title : POWER_I/O_DDR & VTT

Engineer: CH/Fred

Size	Project Name	Rev
Custom	UL50AT	2.0

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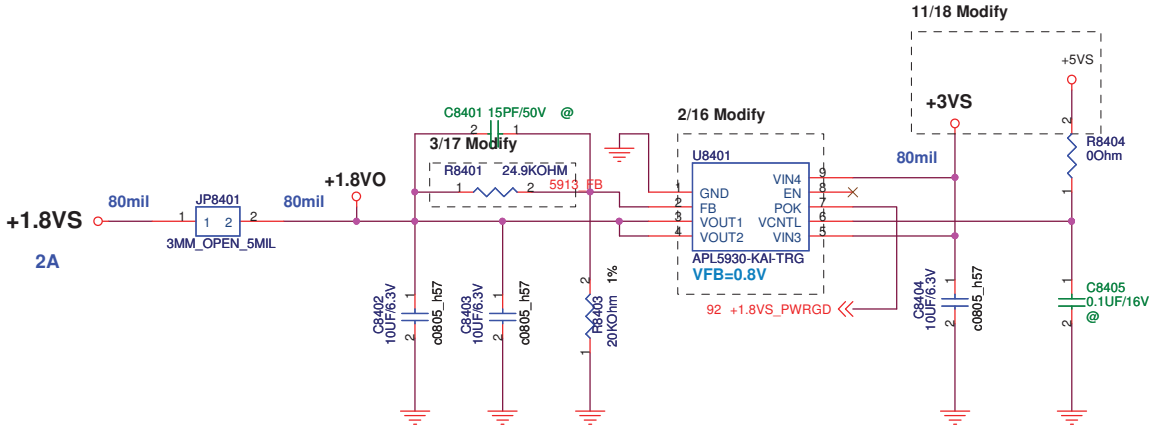
+1.8VS



T8401 TPC28T +1.8VO 1
T8402 TPC28T +1.8VS 1
T8403 TPC28T GND 1
T8404 TPC28T GND 1

<Variant Name>

ASUSTeK COMPUTER INC.	Title : POWER_I/O_ +1.8VS	
	Engineer: CH/Fred	
Size: Custom	Project Name: UL50AT	Rev: 2.0
Date: Friday, October 16, 2009	Sheet 84 of 97	

<Variant Name>

Title : POWER_I/O_VGA

ASUSTeK COMPUTER INC.

Engineer: CH/Fred

Size	Project Name	Rev
B	UL50AT	2.0

Date: Friday, October 16, 2009 Sheet 85 of 97

<Variant Name>

Title : <Title>

ASUSTeK COMPUTER INC.

Engineer: CH/Fred

Size	Project Name	Rev
Custom	UL50AT	2.0

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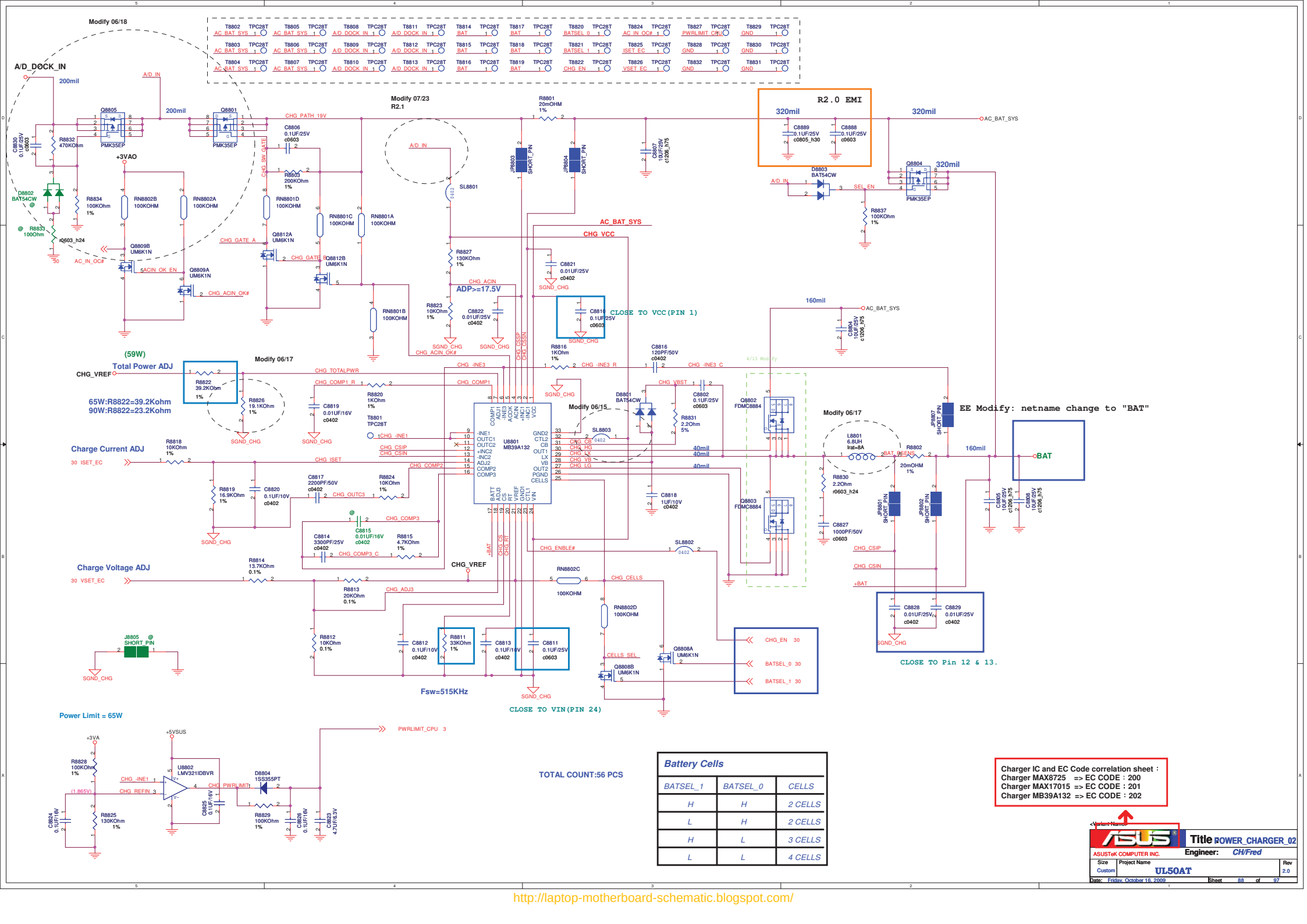
<Variant Name>

ASUSTeK COMPUTER INC.	Title : <Title>	
	Engineer: CH/Fred	
Size: A	Project Name: UL50AT	Rev: 2.0
Date: Friday, October 16, 2009	Sheet 87 of 97	



<Variant Name>

ASUSTeK COMPUTER INC.	Title : <Title>	
	Engineer: CH/Fred	
Size: A	Project Name: UL50AT	Rev: 2.0
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<Variant Name>

ASUSTeK COMPUTER INC.	Title : POWER_DETECT	
	Engineer: CH/Fred	
Size: Custom	Project Name: UL50AT	Rev: 2.0
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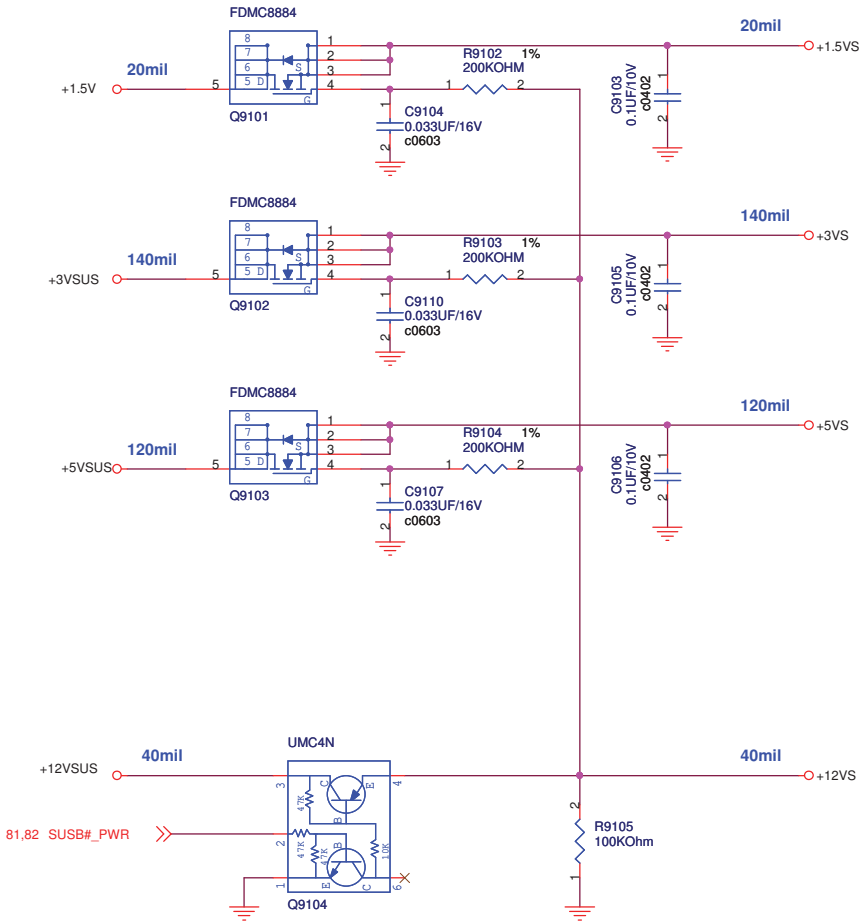
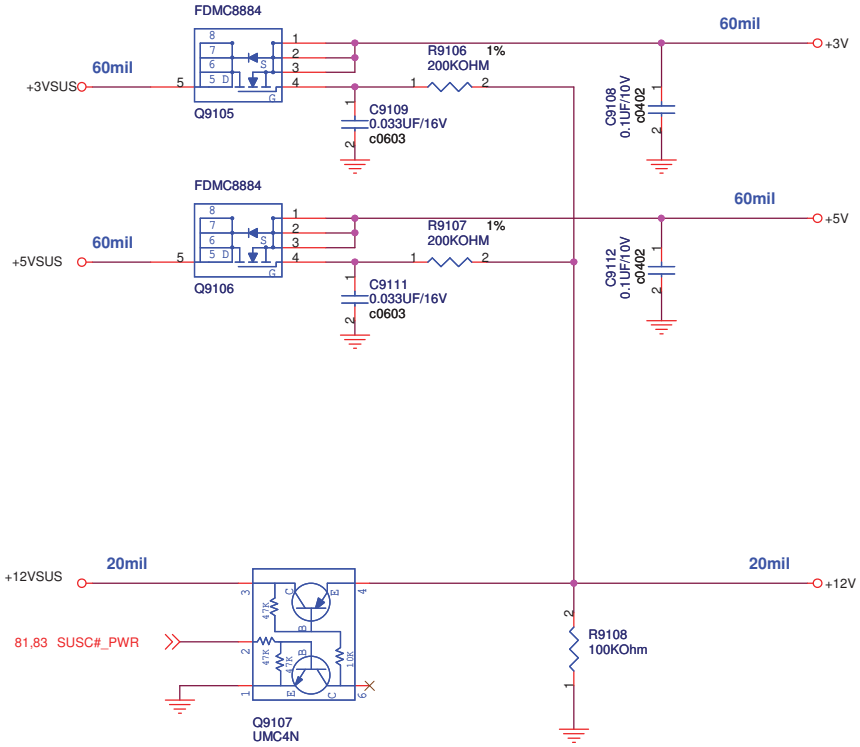
SUSB#_PWR POWER



Total count: 19 pcs

SUSC#_PWR POWER



T9101 TPC28T +12VSUS 1		T9111 TPC28T +3VSUS 1	
T9102 TPC28T +12VS 1		T9113 TPC28T +3VS 1	
T9103 TPC28T +12V 1		T9115 TPC28T +3V 1	
T9104 TPC28T +5VSUS 1		T9120 TPC28T +1.5V 1	
T9106 TPC28T +5VS 1		T9121 TPC28T +1.5VS 1	
T9110 TPC28T +5V 1		T9123 TPC28T SUSB#_PWR 1	
		T9114 TPC28T SUSC#_PWR 1	

<Variant Name>

ASUSTeK COMPUTER INC.	Title : POWER_LOAD SWITCH	
	Engineer: CH/Fred	
Size: B	Project Name: UL50AT	Rev: 2.0
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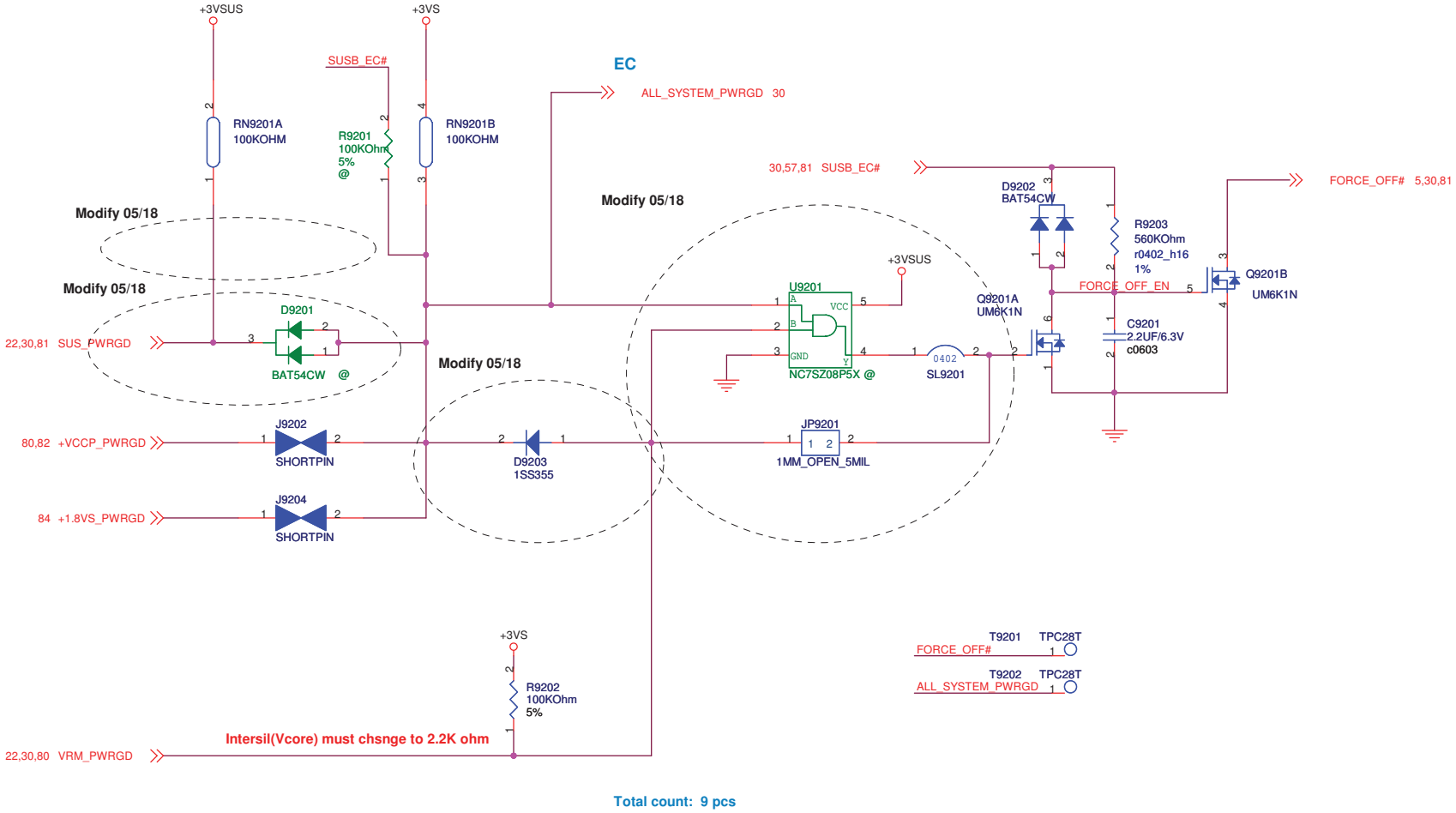
POWER GOOD DETECTER



<Variant Name>

ASUSTeK COMPUTER INC.	Title : POWER_PROTECT	
	Engineer: CH/Fred	
Size: B	Project Name: UL50AT	Rev: 2.0
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<Variant Name>

ASUSTeK COMPUTER INC.	Title : POWER_SIGNAL	
	Engineer: CH/Fred	
Size: Custom	Project Name: UL50AT	Rev: 2.0
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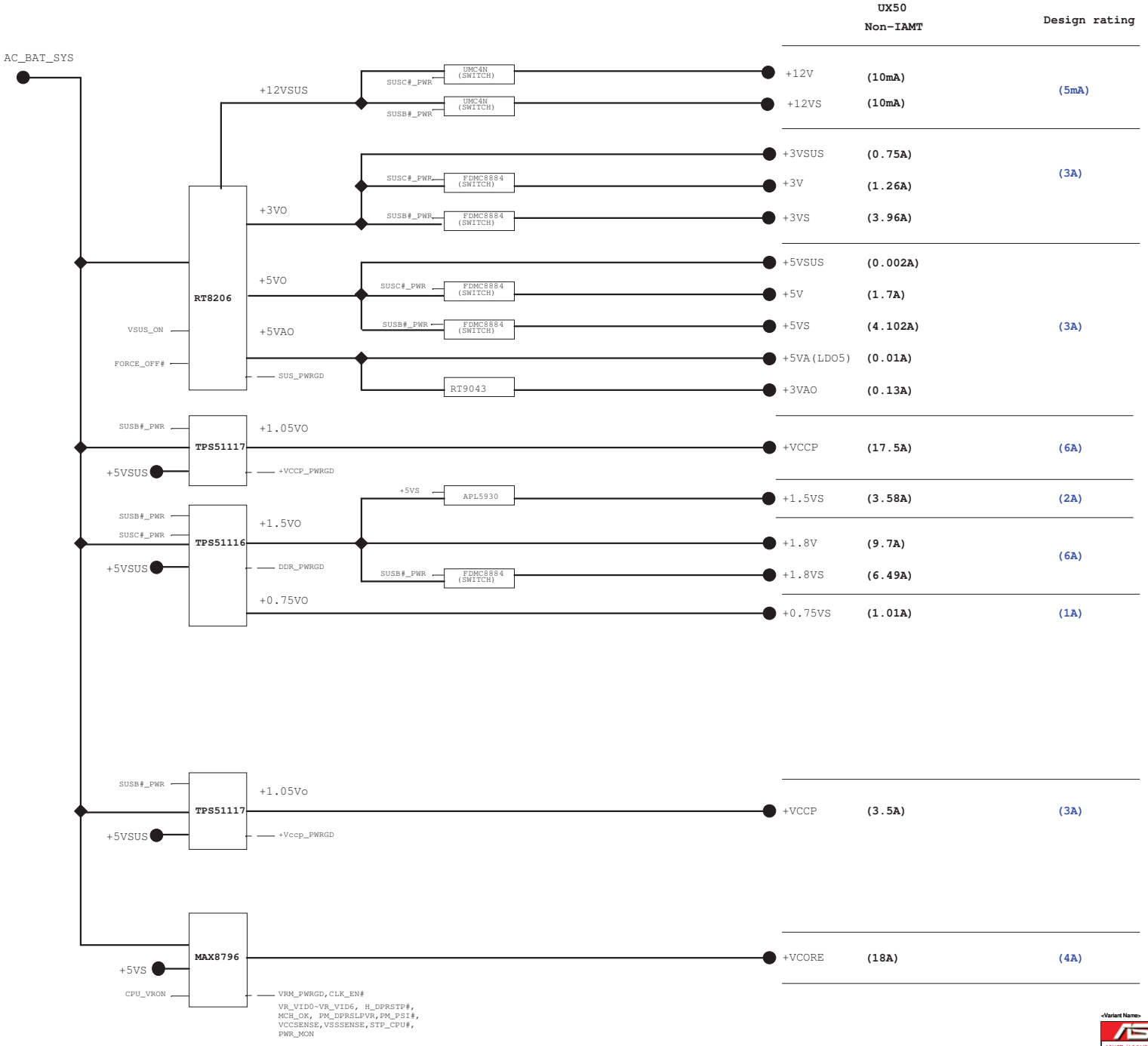

	UX50 Non-IAMT	Design rating
+12V	(10mA)	(5mA)
+12VS	(10mA)	
+3VSUS	(0.75A)	(3A)
+3V	(1.26A)	
+3VS	(3.96A)	
+5VSUS	(0.002A)	
+5V	(1.7A)	
+5VS	(4.102A)	(3A)
+5VA(LDO5)	(0.01A)	
+3VAO	(0.13A)	
+VCCP	(17.5A)	(6A)
+1.5VS	(3.58A)	(2A)
+1.8V	(9.7A)	(6A)
+1.8VS	(6.49A)	
+0.75VS	(1.01A)	(1A)
+VCCP	(3.5A)	(3A)
+VCORE	(18A)	(4A)

<Variant Name>

ASUSTeK COMPUTER INC.

Title : POWER_FLOWCHART

Engineer: CH/Fred

Size: Custom | Project Name: UL50AT | Rev: 2.0

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<Variant Name>

ASUSTeK COMPUTER INC.	Title : <Title>	
	Engineer: CH/Fred	
Size: A	Project Name: UL50AT	Rev: 2.0
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Rev	Date	Description
1.00		First Release!
1.10		
2.00		

<Variant Name>

ASUSTeK COMPUTER INC.

Title : HISTORY

Engineer: Jack Hsu

Size	Project Name	Rev
Custom	UL50AT	2.0

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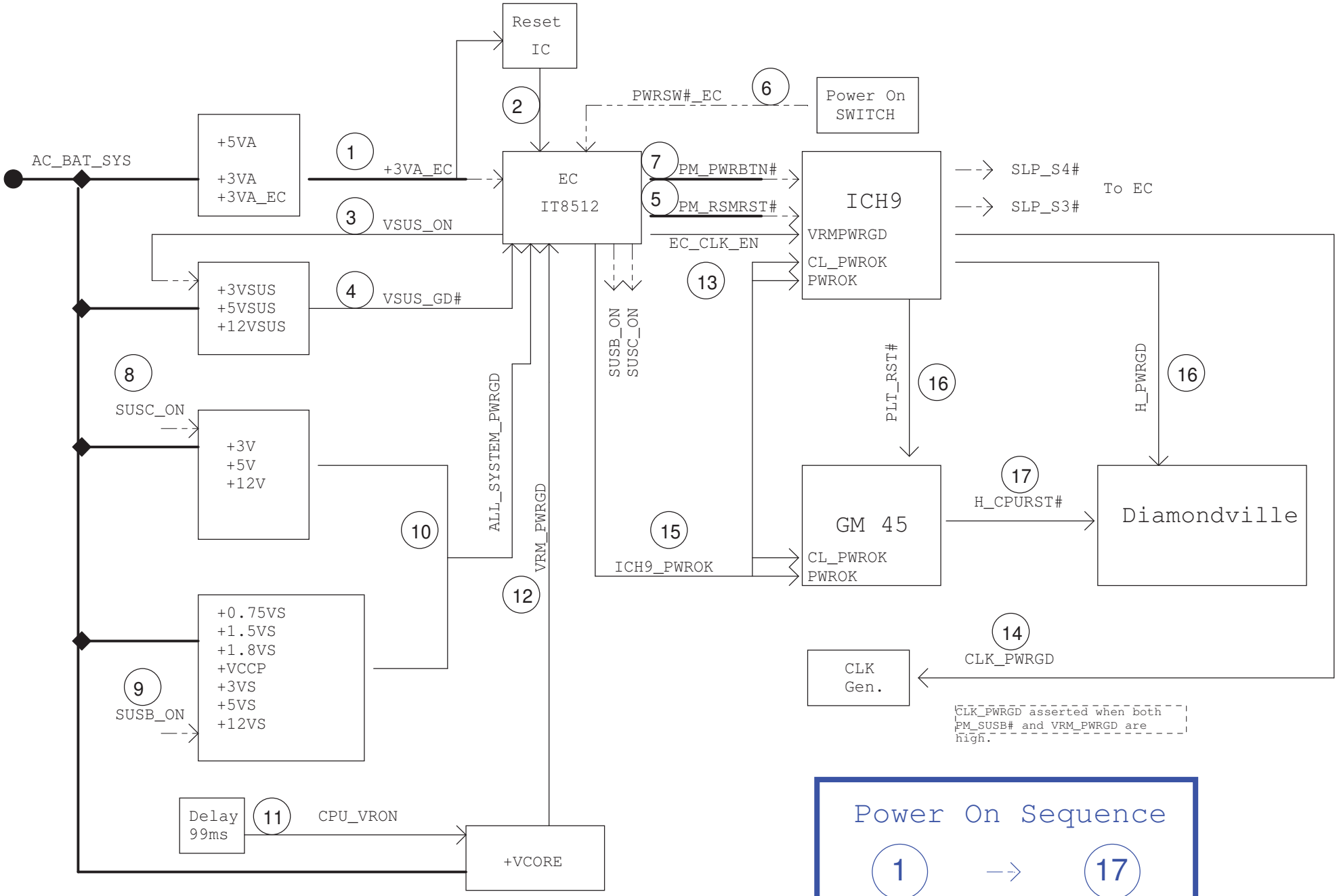

<Variant Name>

ASUSTeK COMPUTER INC.	Title : POWER SEQUENCE	
	Engineer: Eric_Ho	
Size: Custom	Project Name: UL50AT	Rev: 2.0
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